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A High Speed Dynamic Comparator for Ultra High Speed Applications on 70nm Technology

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***Abstract*—The proposed work envisages increasing the sampling frequency of Analog to Digital converts which directly affects their speed while simultaneously decreasing the power consumption which increases the practical applicability of the circuits and renders thermal stability. The low power, high speed and area efficient Analog to Digital Converters (ADCs) use widely dynamic regenerative comparators to maximize their power efficiency, operation speed and area. In this work, a new high clock (sampling frequency) dynamic comparator is proposed based on double tail architecture, where the circuit of a conventional comparator is modified to operate at higher frequencies with reduced energy per conversion (energy required to convert a signal into samples) at low supply voltage. In the proposed comparator, a modification in the form of an extra transistor (control transistor) has been added to the previous circuit along with a reduction in the length of the MOSFET transistor from 180nm to 70nm. This comparator circuit is designed and simulated on the tanner EDA tool. The proposed double tail comparator achieves a minimal energy per conversion of 21pJ and maximum clock frequency up to 3.07GHz at a supply voltage of 1.2V.**

Keywords—High speed ADCs, conventional comparator, Dynamic clocked comparator,

I. INTRODUCTION

Comparator is basic building block for designing of high speed analog to digital converters (ADCs) like flash ADCs. Analog to digital converters (ADCs) require high speed, low power consumption with small chip area. The designing of a comparator can begin with power consumption operation speed and their gains are constrained. The dynamic regenerative comparators are preferred for design of high speed low power ADCs, this is due to the positive feedback strengthen the signal strength in this converter [1][2][3]. A regenerative comparator is shown in fig.1, the basic blocks of a high performance regenerative comparator consist (1) preamplification stage, (2) Regenerative latch Stage or positive feedback stage and (3) postamplification stage or output buffer stage. The input preamplifier stage takes the inputs and amplifies the signals to improve signal sensitivity and feed to input of Regenerative latch or positive feedback stage (i.e amplifies minimum input signal with which the comparator can make a decision). It also isolates the input of the comparator from kickback noise produced during positive feedback stage in the regenerative comparator [10][11]. The decision stage takes amplified input from the preamplifier stage and it determines which of the input signals is large.

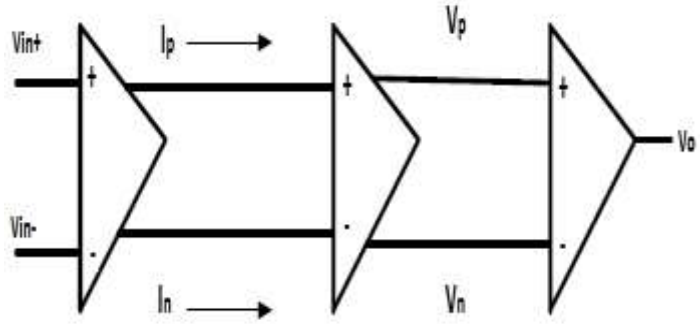

Fig.1 Regenerative Comparator

The preamplifier circuit stage is a differential amplifier and the sizes of its transistors determine the input capacitance and differential amplifier transconductance g_m. The relationship between input voltage and output current *Ip* and *In* is given by

$$I_p=\frac{gm}{2}(V_{in+}-V_{in-})+\frac{Is}{2}=Is-In \quad \text{where } (I_p=-I_n) \qquad (1)$$

The decision stage is very important stage in the comparator and it must be capable to make decision up to mV-level signals. The circuit uses positive feedback to strengthen the signal level to improve the comparator sensitivity [1]. The final stage of the comparator is output buffer or post-amplifier, the main role of this stage is to covert the output of decision circuit into a logic signal (i.e. logic '0' (0V) or logic '1' (VDD)) [3].

III. CONVENTIONAL COMPARATOR DESIGN

A conventional dynamic double-tail comparator is shown in fig.2. This comparator can operate at lower power supply voltages because this topology has less stacking compared to the conventional dynamic comparator. A large current in the latching stage is drawn due to double tails [4].

A. Operation of conventional comparator

The working of this comparator can be understood by transition of clock pulse from reset phase or *CLK* = 0 to *CLK*=1. During reset phase or *CLK* = 0, both tail transistors

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Mtail1, and *Mtail2* are in cut off and the transistors *M3-M4* turn on. *M3-M4* pull up *fn* and *fp* nodes to *VDD*, which in turn causes transistors *MR1* and *MR2* start conducting and these transistors discharge or pull down the output nodes to ground. During decision-making phase when *CLK* =*VDD*, the tail transistors *Mtail1* and *Mtail2* are on and they start conducting, and the transistors *M3-M4* turn off, the voltages at nodes *fn* and *fp* drop with the rate defined by $I_{tail1}/C_{fn(p)}$ and an input-dependent differential a voltage ΔV_f will build up at input of *MR1* and *MR2* which is independent of differential inputs. The intermediate transistors stage *MR1* and *MR2* will pass ΔV_f to the decision circuit and it also provides a good isolation between input and output, which reduces the kickback noise during positive feedback [4].

The delay of this comparator depends on two main parts, the capacitive charging of the load capacitance t_0 and the latch regeneration time t_{latch}.

The delay to of this comparator can be obtained from the equation

$$to = \frac{Vtn\ CL}{IB1} \approx 2\frac{Vtn\ CL}{IB1} \quad (2)$$

Where, C_L load capacitance and IB1 is the drain current of M9

and the latch generation delay of this circuit is given by

$$t_{latch} = \frac{CL}{gm,eff}\ \ln\left(\frac{VDD/2}{\Delta Vo}\right) \quad (3)$$

The total delay of this comparator is achieved as follows

$$t_{delay} = to + t_{latch} \quad (4)$$

$$= 2\frac{Vtn\ CL}{IB1} + \frac{CL}{gm,eff}\ln\left(\frac{VDD/2}{\Delta Vo}\right) \quad (5)$$

From the previous work on conventional comparator, some important notes can be concluded.

1. It has been observed from previous work that at the beginning of the reset phase, the *'outp'* and *'outn'* need to coincide at the same starting voltage point at the outset of the Decision Making Phase. Since during every voltage comparison, voltages *'outp'* and *'outn'* start together and diverge depending upon the stronger value among the two.

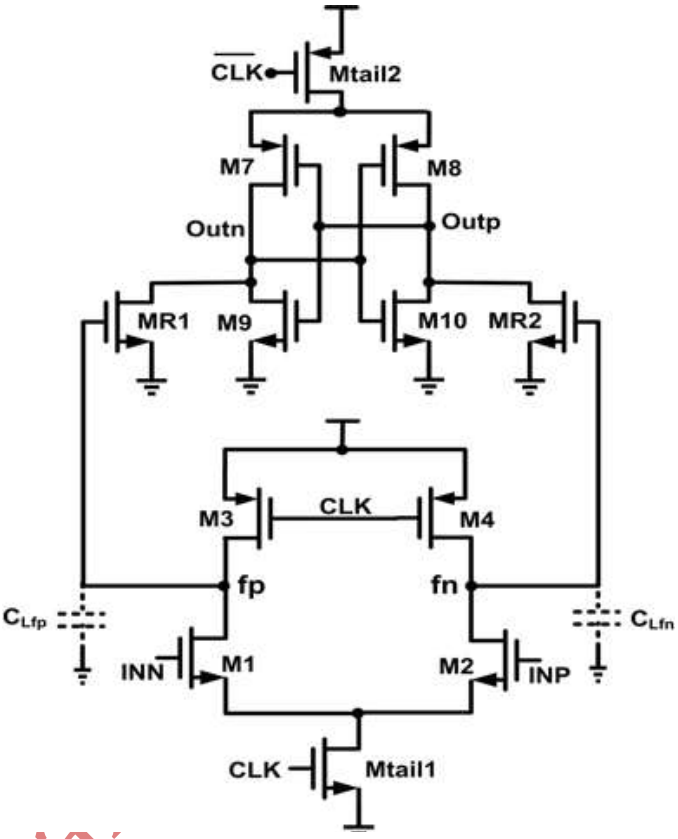

Fig.2 Conventional comparator

Now if we look at the waveforms, we can see time is expended for both the voltage levels to reach the common point at the starting of the reset phase which adversely affects the maximum sampling frequency since time delay results in reduction of frequency.

2. It has been also observed from the previous work that the energy per conversion is comparatively high. This can be understood by the above explanation regarding the delay in coinciding time of outputs *'outp'* and *'outn'*. As the time taken to compare the threshold and the input voltage increases, the energy consumed in that quantum of time also increases which has a detrimental effect on the energy per conversion.

III. PROPOSED COMPARATOR DESIGN

The schematic diagram of the proposed double tail dynamic comparator is shown in fig.3. The proposed dynamic comparator has better performance in low voltage applications. The main idea of the proposed comparator is to reduce exponential decay of comparator circuit during reset phase (the time required to reach both output nodes *'outp'* and '*outn'* at the same potential at initial condition during reset phase) to reduce the delay of comparator, increase sampling frequency and also reduce the energy required by comparator to convert the signal into output samples. For this purpose a small sized transistor (control transistor *Msc*) has been added to the conventional dynamic comparator between the output nodes *'outn'* and *'outp'* [see fig.3].

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The control transistor *MC* reduces the time taken by the both comparator output nodes '*outp'* and *'outn'* to reach at the equal potential during the reset phase, the comparator can operate at higher clock frequency and reduce the delay and energy per conversion of the comparator with improved hysteresis in small supply voltage.

A. *Operation of proposed comparator*

The operation of proposed comparator is as follows (see fig.3). During reset phase when clock pulse is zero (*CLK='0'*) *Mtail1* and *Mtail2* are off and the transistor *M3* and *M4* start conducting which pulls both the nodes *fn* and *fp* to *VDD*. The isolating transistors *MR1* and *MR2* is connected to the *fp* and *fn* nodes respectively due to this, both transistor *MR1* and *MR2* start conducting and they pull both output nodes '*outp'* and *'outn'* to the ground therefore the output '*outp' and 'outn'* nodes discharge to zero. At this state of clock, *Mtail2* is off hence there is no connection between VDD and regenerative latch (decision making circuit) therefore the outputs cannot be pulled to *VDD*. During this phase (*CLK='0'*),the control transistor *MC* is on and it will short both output nodes *'outp' and 'outn'* and bring them at the equal potential .

During decision making phase when clock state is high (*CLK='1'*) the tail transistors *Mtail1*, and *Mtail2* are on, the transistors *M3* and *M4* turn off. Furthermore, at the beginning of this phase, the control transistors *MC* are still on (since *fn* and *fp* are about *VDD*). Thus, *fn* and *fp* nodes start to drop to ground with different rates according to the input voltages (*INN* and *INP*). Suppose *INN* > *INP*, thus *fp* drops faster than *fn*, because transistor *M1* provides more current than *M2*.

As long as *fp* will fall faster than *fn* the intermediate transistor *MR1* will start to turn off faster than the *MR2*, at this clock state *Mtail2* is on, will charge the decision making circuit to *VDD*. As long as the transistor *MR1* turning off faster than *MR2* therefore after sometime transistor *MR1* turn off completely while transistor *MR2* still discharging to ground therefore the transistor *MR1* is isolated first to the decision circuit while transistor *MR2* still charging.

The output node *'outn'* is completely isolated from the transistor MR1 and charge to VDD , the transistor M8 turn off and transistor M10 starts conducting and discharge the output node *'outp'* to the ground at this time the control transistor MC is in cut off or it acts as open switch (during decision making phase; CLK=1). When clock pulse changes its state from CLK=1 to CLK=0, the control transistor *Msc* start conducting hence one of the output node (outn) which is at higher potential is pulled down while the other node (outp) is pulled up. When clock pulse changes its state completely to zero, the control transistor acts as a short circuit and provide a short circuit between output nodes *'outn'* and *'outp'* both output nodes *'outn'* and *'outp'* therefore the potentials at *'outn'* and *'outp'* are equal which results reducing in final exponential decay period.

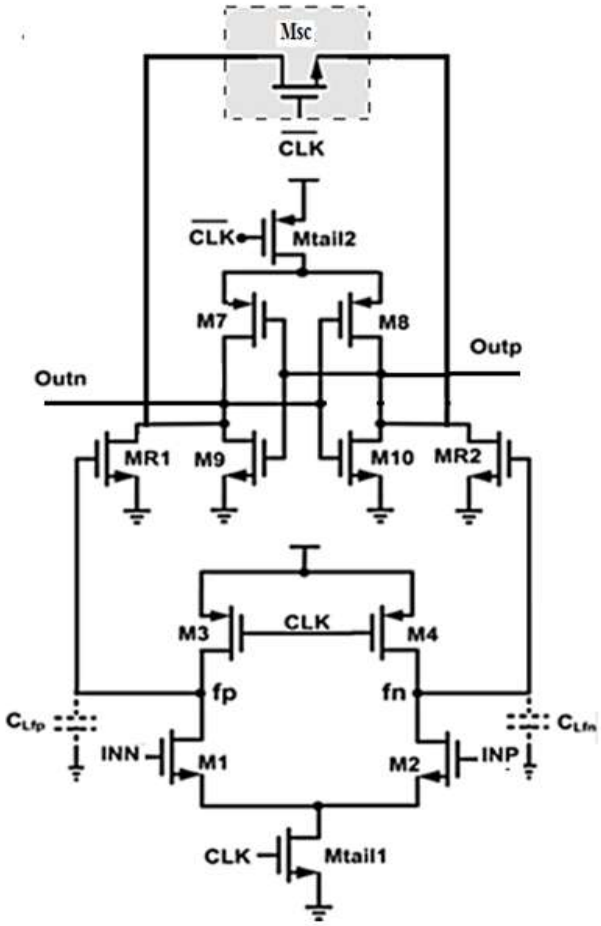

Fig.3. Proposed dynamic comparator

IV SIMULATION RESULTS

The proposed comparator comparing with the conventional double-tail dynamic comparators circuit has been simulated in a 70nm CMOS technology using tanner EDA with *VDD* = 1.2 V. The simulation waveform of proposed comparator is shown in fig.4. The maximum frequency of the proposed comparator is observed 3.07GHz and energy per conversion of 0.21pJ with input supply *VDD* = 1.2V

A. *Maximum Clock frequency*

The value of maximum sampling frequency has increased from 2.4 GHz up to 3.07 GHz. This substantial increase can be attributed to the design of the circuit of the comparator. As we can see from the circuit of the proposed comparator, the two output terminals viz. '*outp'* and '*outn'* have been shorted through the MOSFET Controlled Transistor (*Msc*). Now, from the functioning of the Comparator circuit without *Msc*, we observe that a condition of race occurs between the two transistors '*outp'* and '*outn'* respectively during the decision making stage finally culminating to the reset stage. The major issue affecting the Maximum Sampling Frequency is the delay period after which the outputs of both the transistors '*outp'* and

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'*outn'* reach a common voltage level of zero volts. As the outputs of both the transistors shoot towards opposite voltage polarities initially during the decision making stage, reaching the common zero potential results in expenditure of time, thus adversely affecting the frequency (rather the maximum sampling frequency). This effect was indispensible from the previous method since transistors, no matter how similar show variations in performance as fabricating two exactly identical transistors are practically impossible. Our approach was to mitigate this by finding a way around the above mentioned problem. Shorting the outputs '*outp'* and '*outn'* results in pulling up the voltage level of the transistor having a lower voltage and pulling down the voltage level of the transistor having a higher voltage. It should be noted though that which transistor would be at a higher voltage level is an unpredictable phenomenon, depending upon the outcome of the race between the outputs of the two transistors. But this phenomenon of pulling up and pulling down doesn't need both the transistors to reach a common Zero Voltage Level rather it begins the reset state as soon as both transistors reach a Common Voltage Level. As it can be inferred or even seen from Fig 5.3 that it takes lesser time for both the transistors to reach a common voltage level as they don't need to traverse the Entire Dynamic Range between the high and low voltage levels. This effect considerably reduces the sampling time thereby bringing about a substantial change in the Maximum Sampling Frequency**,**

B. Reducing energy per conversion

It is not only the speed parameter which is improved in the modified proposed Comparator, but the energy per conversion is reduced as well. The energy per conversion has been reduced from 0.24 Pico Joule to 0.21 Pico Joule. The reduction can be explained as: The energy per conversion crucially depends upon the time needed for the conversion. Lesser the time for conversion, lesser is the energy expenditure. Thus we can see that the energy per conversion depends on the maximum sampling frequency. Since the maximum sampling frequency in the proposed model has reduced, therefore the energy per conversion has also reduced.

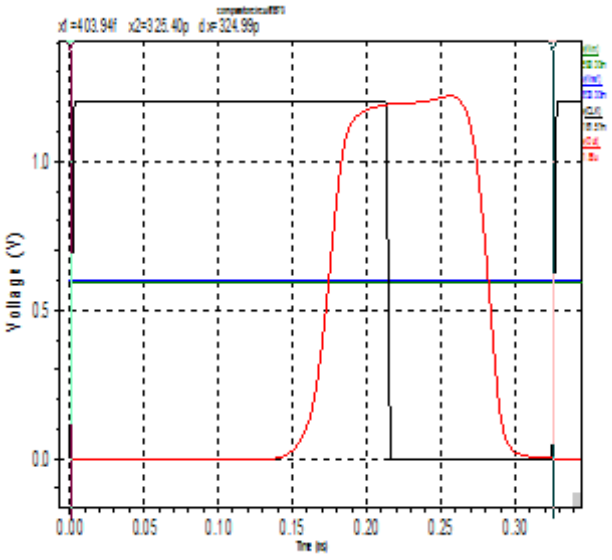

Fig.4 Simulation waveform of proposed comparator with VDD=1.2V

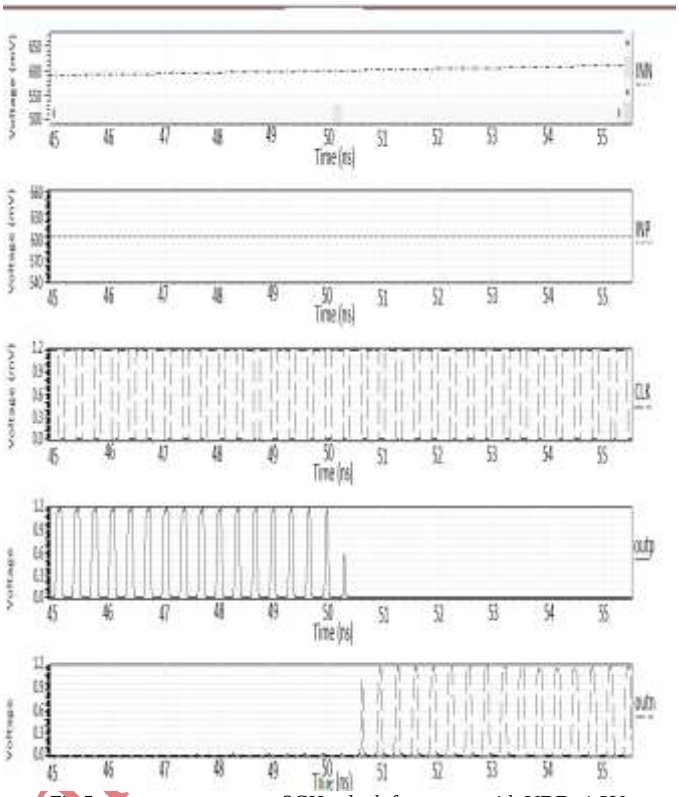

Fig.5 comparator output at 3GHz clock frequency with VDD=1.2V

The fig.5 shows simulation waveform of output nodes *'outp'* and *'outn'* with VDD =1.2V, in comparison with the previous structure (Double tail comparator), the output of the proposed double tail comparator is improved at increased clock frequency compared to Conventional comparator in low voltage supplies.

Table I
Performance Comparison

Comparator structure	**Conventional Dynamic Comparator**	**Single Clock Dynamic Comparator**	**Proposed Dynamic Comparator**
Technology CMOS	180nm	180nm	70nm
Supply Voltage	0.8V	0.8V	1.2V
Maximum Sampling frequency	1.8GHz	2.4GHz	3.07GHZ
Energy per conversion	0.27pJ	0.24pJ	0.21pJ

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V. CONCLUSION

In this paper, a comparator circuit based on shorting transistor (Msc) structure has been investigated for high-speed ADCs. Introducing the Control Transistor (*Msc*) in the circuit has improved the performance of the circuit. The maximum sampling frequency has increased from 2.4 GHz to 3.07 GHz, the energy per conversion has reduced from 0.24 Pico Joule to 0.21 Pico Joule. The reduction in energy per conversion can be attributed to the fact that the technology used in the proposed model is 70nm compared to 180nm used earlier and the sampling frequency has increased from 2.4GHz to3.07GHz. Reduction in size reduces the energy per conversion. Increasing the maximum sampling frequency reduces the time per conversion which reduces the energy per conversion. The improvements are believed to substantially improve the performance of ADCs for which comparators are designed as the maximum sampling frequency and energy per conversion are the parameters of paramount importance which finally decide the practical applicability of such circuits.

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