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An Optimized Higher Order Sigma Delta Modulator Using Multi bit Quantizer

Mr. Raju Premlal Yadav
M.Tech Scholar
LKCT, Indore
Yadavraju185@gmail.in

Mr. Deepak Sharma
Asst. Professor
LKCT, Indore
Deepaksharma2189@rediffmail.com

***Abstract*— This paper presents the fundamentals of Analog to Digital Conversion using the Sigma Delta Modulation concept. It has been clearly shown how the process of Sigma Delta Conversion used in ADCs can achieve higher speeds even after employing Oversampling above Nyquist rate. The various parameters affecting the design and performance of the Delta Sigma employed ADC have been analyzed. Stability considerations of higher order sigma delta modulators have also been analyzed to attain an optimized approach to decide upon the**

Keywords—Delta Sigma, Analog to Digital Converter (ADC), Over Sampling Rate (OSR), Dynamic Range (DR).

I. Introduction

Although real world signals are analog, it is often desirable to convert them into the digital domain using an analog to digital converter (ADC). Signal processing in the digital domain is useful in digital storage, biomedical applications, and industrial applications - from instrumentation to communication. Sigma Delta Modulators achieve a high degree of insensitivity to analog circuit imperfections, thus making them a good choice to realize embedded analog-to-digital interfaces. Application based and sophisticated design techniques demand Radio Frequency Identification Techniques which find its application in object tracking, etc. Sigma Delta ADC is high resolution ADC and acts as a major building block in RFID applications. [1] As per the sampling frequency, ADC is classified into two categories: Nyquist ADCs and Sigma- Delta ADCs. Nyquist ADCs have a lower effective number of bits due to process variation and mismatching [2]. One technique, Sigma Delta modulation, which is based on the combination of oversampling and quantization error shaping techniques, has become quite popular for achieving high resolution and high accuracy. [3] One significant advantage of the method is that analog signals are converted using only a 1-bit ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. Using sigma-delta A/D methods, high resolution can be obtained for only a low to medium signal bandwidths. The Oversampling behavior of the Sigma Delta Modulator restricts the bandwidth which can be overcome by using higher order architecture.

The Signal to Noise Ratio of Sigma Delta Modulator is dependent upon the number of bits of quantizer and is independent of amplitude of input signal. The N - bit quantizer has 2 levels and separated by V LSB. The amplitude of full scale sine wave input is 2^{N-1} V LSB. Peak to peak value is given by 2^{N} V LSB Mean Square Value of the Signal is given by:

$$S = (2^{N-1}V_{LSB})^{2} / 2 \quad (1)$$

Mean squared Noise is given by the expression:

$$N = V^{2}_{LSB}/12 \quad (2)$$

Therefore,
Signal to Noise Ratio (SNR) is given by:

$$[(2^{N-1}V_{LSB})^{2} / 2] / [V^{2}_{LSB}/12] \quad (3)$$

which reduces into

$$SNR=12^{2N} \quad (4)$$

Also,

$$SNR = 6.02\,N + 1.76\text{ dB} \quad (5)$$

II. PRINCIPLE OF OPERATIONBEHIND SIGMA DELTA MODULATORS

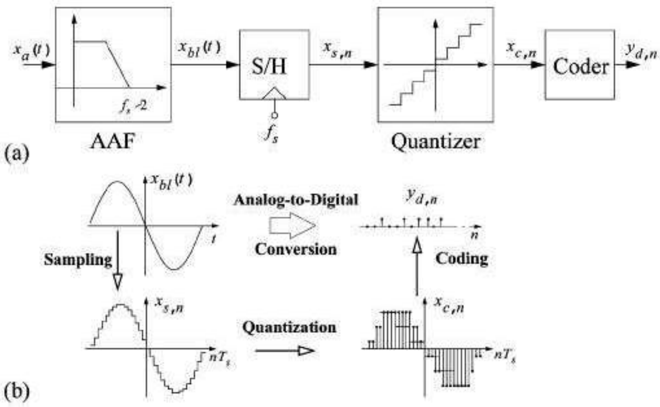

Fig.1 Block Diagram of Sigma Delta Modulators

The operation of Ms relies on the combination of two signal processing techniques, namely: oversampling and quantization error filtering and feedback, commonly referred to as noise shaping. Both techniques are related to the fundamental processes involved in an ADC—illustrated in Fig. 1(a) shows the conceptual scheme of an ADC intended

for the digitization of low-pass (LP) signals, that includes
the following components: an anti-aliasing filter (AAF), a
sampling-and-hold (S/H) circuit, a quantizer, and a coder
The operation of these blocks is illustrated in Fig. 1(b). First,
the analog input signal, , passes through the AAF block.
Otherwise, from the Nyquist sampling theorem, high frequency components of the input signal would be folded or aliased into the signal bandwidth, , thus corrupting the signal
Information.

III OVERSAMPLING

The sampling process imposes a limit on , and hence on
the speed of the ADC. According to the Nyquist theorem, which sets that the minimum value of —often referred to as Nyquist frequency and represented by —must be twice the signal bandwidth, i.e., . Based on this criterion, those ADCs
with are called *Nyquist-rate* ADCs, while if, the resulting ADCs are known as *oversampling* ADCs, and OSR is defined as the *oversampling ratio*. One of the advantages of oversampling ADCs is that they simplify the requirements placed on the AAF as illustrated in Fig.2. It should be kept in mind that the AAF for a Nyquist converter must have a sharp transition band, which often introduces phase distortion in signal components located near the cut-off frequency.

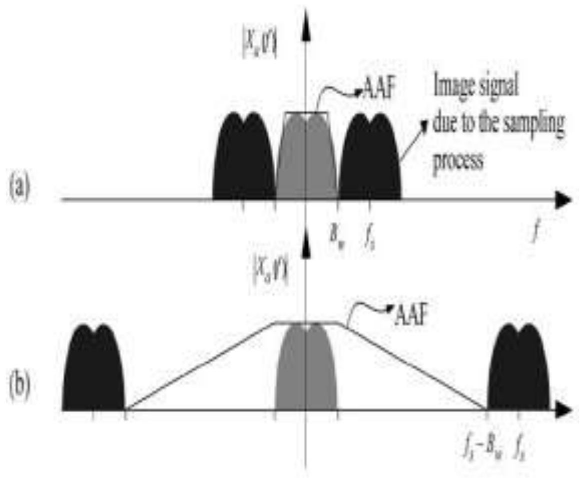

Fig.2 Oversampling using the AAF

IV QUANTIZATION ERROR AND WHITE NOISE MODELLING

The quantization itself introduces a fundamental limitation
on the performance of an ideal ADC. It degrades the quality
of the input signal whose continuous-value levels are mapped
onto a finite set of discrete levels as illustrated in Fig. 3. This
continuous-to-discrete transformation in amplitude generates an error, commonly referred to as *quantization error*. Contrary to the sampling process, quantization is a non reversible operation, causing a loss in the *resolution* of the digitized signal .Fig. 3 shows the transfer characteristic of an ideal quantizer ,where denotes the slope of the line intersecting the code steps or quantizer gain, and stands for the quantization error.

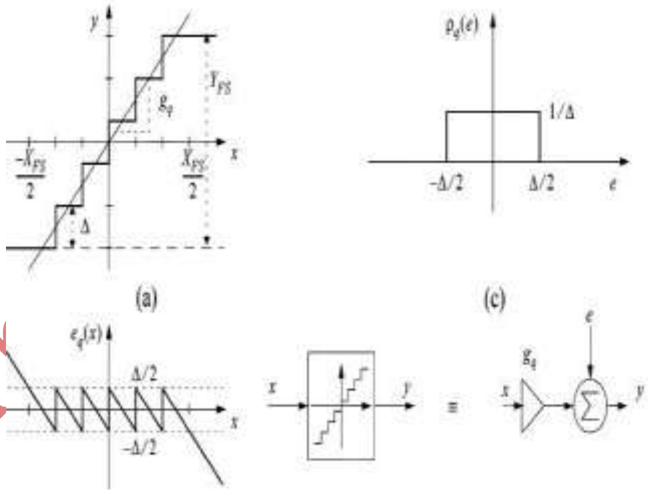

Fig.3 QUANTIZATION ERROR AND NOISE MODELLING

V. SIMULATION RESULTS

This section will deal with the comparative analysis of fourth order Sigma Delta Modulator with respect to different topologies for parameters like signal to noise ratio and effective number of bits. For realization initial parameters are taken for all topologies as OSR = 4, out of band gain (OBG) = 1.5, Quantization Level=7. A comparison of different parameters is done for different values of OSR. For the CIFB topology, Figure 5.12 gives the Realization of STF and NTF in voltage, Figure 5.13 shows the Realization of STF and NTF in dB, Figure 5.14 shows the time domain simulation of fourth order Sigma Delta Modulator , Figure 5.15 shows the integrator states of fourth order Sigma Delta Modulator where x1 is the output of first integrator, x2 is the output of second integrator, x3 is the output of third integrator, x4 is the output of fourth integrator and Figure 5.16 shows the frequency domain simulation of fourth order Sigma Delta Modulator.

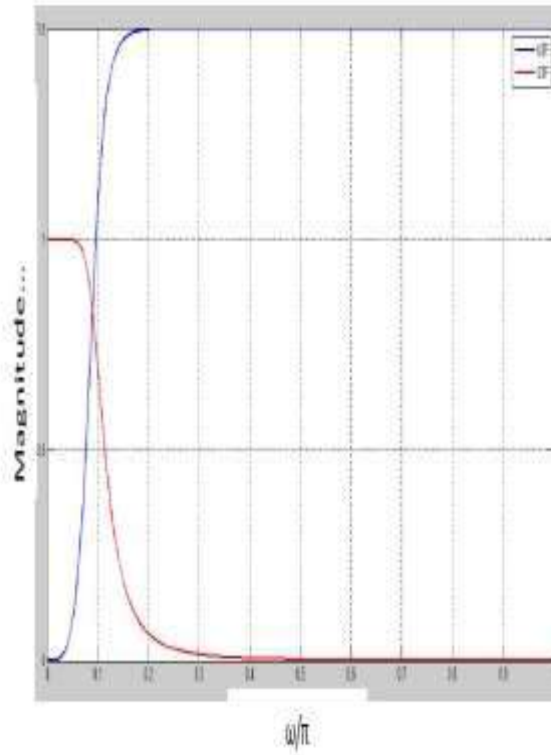

Fig.4 REALIZATION OF STF AND NTF IN VOLTAGE

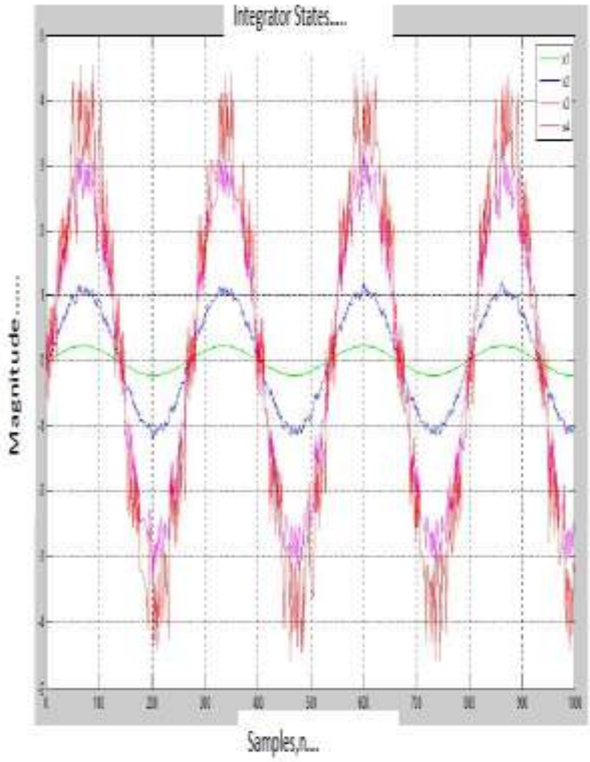

FIG.6 INTEGRATOR STATES OF FOURTH ORDER SIGMA DELTA MODULATOR WITH CIFB ARCHITECTURE

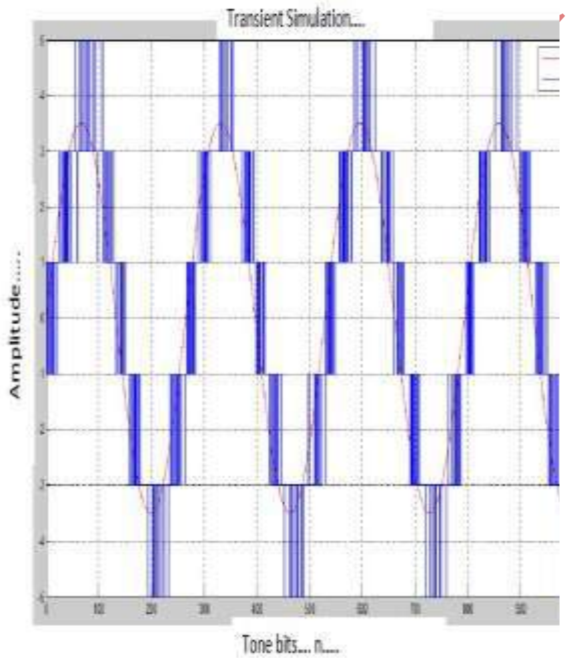

FIG.5 TIME DOMAIN SIMULATION OF FOURTH ORDER SIGMA DELTA MODULATOR WITH CIFB ARCHITECTURE

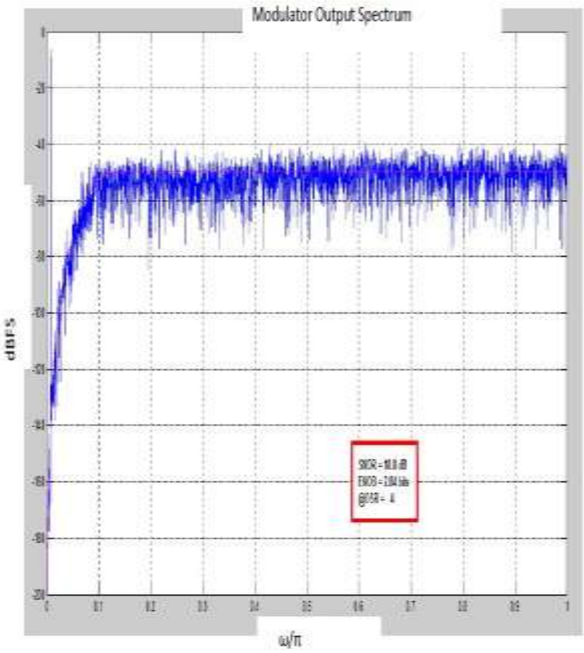

FIG.7 FREQUENCY DOMAIN SIMULATION OF FOURTH ORDER SIGMA DELTA MODULATOR WITH CIFB ARCHITECTURE

Sr. No.	OSR	SNR	ENoB
1	2	14.1	2.04
2	4	18.8	2.84
3	8	25.7	3.98
4	16	47.1	7.53
5	32	74.3	12.05
6	64	103.6	16.92
7	128	137.4	22.53

TABLE.1 ANALYSIS OF FOURTH ORDER SIGMA DELTA MODULATOR FOR SIGNAL TO NOISE RATIO AND EFFECTIVE NUMBER OF BITS.

Thus the aforesaid discussions along with the relevant waveforms and tables are self explanatory for the performance of higher order sigma delta modulators. The above comparative analysis concludes that parameters affecting the performance of Sigma Delta Modulator like Signal to Noise Ratio and Effective Number of Bits increases with increase in Over Sampling Ratio. Also, with the increase in order of modulator and quantization level, high SNR can be achieved at low OSR value. But with the increase of order, the modulator becomes unstable and also, maximum usable input signal amplitude decreases. The stability can be achieved for high order Sigma Delta Modulator by keeping the gain of Noise Transfer Function to be low. So, low order Sigma Delta Modulator with high OSR can be used for application.

By the use of uniform quantizer, the performance of Sigma Delta Modulator increases drastically. Stability issues can be resolved by using multibit quantizers. But the designing of multibit quantizer is complex. Also its implementation in chip is quite cumbersome, with respect to large scale integration technologies. The stability of loop filter depends upon number of factors like maximum input signal range, position of poles of Noise Transfer Function in unit circle, gain value of the loop filter etc.

So, by considering all the above parameters as per the application, the Sigma Delta Modulator of specific architecture with required order can be used. If the bandwidth requirement is modest, then conventional model of Sigma Delta Modulator of low order can be used. The Analog to Digital Converters required for audio signals which are having higher bandwidth can use Sigma Delta Modulator of higher order.

VI CONCLUSION

In this work, analysis of lower order and higher order Sigma Delta Modulator has been done on the basis of Signal to Noise Ratio and Effective Number of Bits. The noise shaping property of Sigma Delta Modulator has made it popular in the application where high Signal to Noise Ratio is desired. The significant property of noise shaping, pushes the noise in the range out of band of interest which reduces the requirement of sharp cut off anti aliasing filter. As, the oversampling ratio increases the Signal to Noise Ratio also increases. Higher SNR values can be achieved at lower OSR also, if higher orders of modulators are used. But as the number of integrators in the modulator increases this affects in the position of poles of the Noise Transfer Function which can make the loop filter unstable. It can be concluded from the results and conclusions that the sigma delta scheme is a highly efficient technique that can be utilized for the design of Analog to Digital Converters which yield low Quantization Noise due to the noise shaping principle employed inherently in the proposed technique.

REFERENCES

[1] Yingqi Qian Changchun Zhang a, Zhongchao Liu, Leilei Liu, YurongLuan,Yuming Fang and Yufeng Guo,“ *A High-Performance Sigma-Delta Modulator in 0.18pm CMOS Technology”* International Journal, Applied Mechanics and Materials Vols. 519-520 (2014) pp 1085-1088, February 2014

[2] Fan Wenjie ,LvQiuye,HeChong,YinLiang,LiuXiaowei, *“Architectural Design and Simulation of A Fourth-Order Sigma-Delta Modulator ”* , International Journal, Key Engineering Materials Vols. 609-610 (2014) pp 723-727 , April 2014

[3] Hetal Panchal, *“Design and Simulation of Sigma Delta ADC Using VHDL AMS”* , International Journal of Engineering Development and Research , Volume 2, Issue 1 ,pp no.548-551, 2014

[4] Liu Liang, Chen Song , He Chong, Yin Liang, Liu Xiaowei *“Design of Third-order Single loop Full Feed-forward Sigma Delta Modulator*”, International Journal, Key Engineering Materials Vols. 609-610 (2014) pp 1176-1180, April 2014

[5] RaminZanbaghi, Pavan Kumar Hanumolu “An *80-dB DR, 7.2-MHz Bandwidth Single OpampBiquad Based CT Modulator Dissipating 13.7-mW* ”, IEEE Journal of Solid-State Circuits, Vol. 48, No. 2, pp 1 -15, February 2013

[6] Jiandong Cheng, Guoyong Shi, and Ailin Zhang, *"A Fast SNR Estimation Method for Sigma-Delta Modulator Design"* , TENCON 2013, IEEE Conference, 22nd -25th October ,pp 1-4, 2013

[7] Philip M. Chopp and Anas A. Hamoui, *"A 1-V 13-mWSingle-Path Frequency-Translating AZ Modulator With 55-dB SNDR and 4-MHz Bandwidth at 225 MHz"* , IEEE Journal of Solid-State Circuits, Vol. 48, No. 2, pp 1-14 February 2013

[8] HisatoFujisaka , Takeshi Kamio, Chang-Jun Ahn, Masahiro Sakamoto, and Kazuhisa Haeiwa "*Sorter-Based Arithmetic Circuits for Sigma-Delta Domain Signal Processing—Part I: Addition, Approximate Transcendental Functions, and Log-Domain Operations*", IEEE Transactions On Circuits and Systems—I: REGULAR PAPERS, Vol. 59, No. 9, ,pp no. 1952-1965, September 2012

[9] Jose M. de la Rosa, " *Sigma Delta Modulators : Tutorial Overview, Design Guide, and State of the Art Survey ",* IEEE Transaction on Circuits and System - I , Vol 58 No. 1, pp 121, January 2011

[10] Philippe Benabes, Catalin-Adrian TUGUI, "Effective Modeling Of CT Functions For Fast Simulations Using MATLAB-Simulink And VHDL AMS applied to Sigma-delta Architectures" Circuits and Systems (ISCAS), IEEE Conference, Page No. 2269 - 2272 , May 2011

[11] Valeri Mladenov , "*A Method for Validation the Limit Cycles of High Order Sigma-Delta Modulators*" , IEEE Conference , Nonlinear Dynamics and Synchronization (INDS) & 16th Int'l Symposium on Theoretical Electrical Engineering (ISTET), 2011 Joint 3rd Int'l Workshop , pp 1-5, 25-27 July 2011

[12] JozefMihalov, VieraStopjakova ,"*Implementation of Sigma-delta Analog to Digital Converter in FPGA",* IOP, Applied Electronics, IEEE Conference , Page No. 1-4, Sept. 2011

[13] Ahmed Shahein, Mohamed Afifi, Markus Becker, NiklasLotze, YiannosManoli, *"A Power- Efficient Tunable Narrow-Band Digital Front End for Bandpass Sigma—Delta ADCs in Digital FM Receivers*'", Circuits and Systems II: Express Briefs, IEEE Conference ,Vol. 57,Issue No. 11, pp 883 -887, November 2010

[14] Philippe Benabes, Ali Beydoun, Mohamad Javidan, *"Frequency-band-decomposition Converters Using Continuous-time Sigma-Delta A/D Modulators",* Circuits and Systems and TAISA Conference, IEEE Conference, Page No. 1-4, July 2009

[15] Tao Wang and Liping Liang, " *Analysis and Design of a Continuous-Time Sigma-Delta Modulator with 20MHz Signal Bandwidth, 53.6dB Dynamic Range and 51.4dB SNDR"* , 4 IEEE International Symposium on Electronic Design, Test and Applications, page no. 79-84, 2008

[16] Jesus Arias, Peter Kiss, *Member*, Vladimir Prodanov, Vito Boccuzzi, Mihai Banu, David Bisbal, Jacinto San Pablo, Luis Quintanilla and Juan Barbolla, *"A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers*" , IEEE Journal of Solid-State Circuits, VOL. 41, NO. 2, pp no. 339 -351, February 2006

[17] Matthias Keller , Alexander Buhmann, Jens Sauerbrey, MauritsOrtmanns and YiannosManoli "*A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma—Delta Modulators'"* IEEE Transactions on Circuits and Systems— I: Regular Papers, Vol. 55, No. 11,pp no.3480-3487, December 2008

[18] J. Silva, U. Moon, J. Steensgaard and G.C. Temes" *Wideband Low-distortion Delta-Sigma ADC Topology",* Electronics Letters, IEEE Conference, Vol. 37, Issue : 12 , Page No. 737 - 738, Jun 2001

Books

[19] Richard Schreier and Gabor C. Temes , " **Understanding Sigma Delta Data Converters**" ,IEEE Press, A John Wiley& Sons, Inc., Publication, Hoboken, NewJersey , 2005

[20] Steven R. Norsworthy, Richard Schreier and Gabor C. Temes" *Delta Sigma Converters, Theory Design and Simulation"* IEEE Press, IEEE Circuits and System Security, New York, 1997

[21] S.K. Mitra , " *Digital Signal Processing- A Computer Based Approach",* McGraw - Hill, 3rd Edition, India, 2008