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A LOW POWER,LOW PHASE NOISE CONTRIBUTION MOSFET 29 GHz CMOS LC VCO USING 65 nm TECHNOLOGY

VIKETAN VERMA
viketanv17@gmail.com
VITM-INDORE(M.P.)

JITENDRA SINGH DODIA
jitendra.dodiya@vitmindore.com
Asst. Prof. ,VITM-INDORE(M.P.)

Abstract: An increased demand for multi-band and multi-standard radio-frequency (RF) systems requires a voltage controlled oscillator (VCO) operating over a wider frequency range. In a communication system, the VCO is generally used in a PLL (phase-locked loop) or a frequency synthesizer and therefore plays an important role. So the power requirement for VCO and phase noise contribution by mosfet's in VCO will be important parameter to be monitored.

This work presents the design and simulation of CMOS LC VCO in Tanner EDA tool for 65nm CMOS technology process. This work give the tuning frequency of circuit is from 27 GHz to 32.5 GHz that can obtain by applying tuning voltage ranging from 0 V to 1 V. The proposed VCO dissipates power of 500 uW at the maximum oscillation frequency which is very low compared to VCO implement by other publications. This paper also shows that phase noise contribution by mosfet's is very less as compared to the other papers.

I. INTRODUCTION

Voltage Controlled Oscillator is tunable oscillator whose output frequency islinear function of control voltage. The relation between output frequency (f0) and controlvoltage Vconis given below

$$fout = f0 + KV.Vcon$$

Where, *f*0 is the oscillation frequency at $Vcon = 0$ and $KVCO$represent the gain or sensitivity of the circuit . The achievable range, *f2 – f1*, is called the frequency tuning range.

The VCO can easily tuned by charging the capacitor of tank through the use of a voltage depended capacitor which is varactor. There are two types of varactor are available one is reverse bias PN junction diode and other is MOS varactor.

LC VCO consist tank circuit and active element. This tank circuit consist parallel combination of an inductor and a capacitor. The oscillator tank resonate at frequency ω0 is given below

$$\omega 0 = 1/\sqrt{LC}$$

But element of tank circuit, inductor and capacitor offered a series resistance and other parasitic.

1.1 Characteristics of VCO

a) Phase Noise: In LC oscillator noise is mainly injected by active transistor and passive element. The noise mainly affects both amplitude and frequency of LC oscillator. But amplitude noise does not critically affect oscillation because non linearity of oscillator limits the amplitude noise. Noise in phase is referred as phase noise which is basically a random deviation in frequency or random variation in zero crossing point of time dependent oscillator waveform.

David B. Lesson in 1966 given a phase noise model commonly known Lesson's model for oscillator the phase noise predicated by this model is can be expressed as

$$L(\Delta\omega) = 10\log\left[\frac{2FK_T}{P_s}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right]$$

By choosing carefully power supplies, power supply noise and tuning voltage supply noise can be minimized. Due to this reason phase noise of the VCO is mainly determined by the overall quality factor Q of the circuit.

b)Tuning Range: Frequency of oscillation for LC tank is given below by manipulating equation

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

By above equation it's clear that tuning of an oscillator is achieved by varying the values of inductor and capacitor of tank circuit. LC VCO basically tuned by varying the value of capacitor of tank circuit because active inductor show poor phase noise characteristics. Tuning of capacitor is achieved by use of voltage dependent capacitor which is varactor. By varying the voltage of these varactor maximum and minimum capacitance can be obtained which help to calculate minimum and maximum oscillation frequency which is given by below equations

$$f_{max} \approx \frac{1}{2\pi\sqrt{LC_{min}}}$$

$$f_{min} \approx \frac{1}{2\pi\sqrt{LC_{max}}}$$

The C_{max}/C_{min} is necessary for designing LC VCO which is given by below equation

$$\frac{C_{max}}{C_{min}} = \frac{f^2{}_{max}}{f^2{}_{min}}$$

Where centre frequency of oscillation f_0 is given by below equation

$$f_0 = \frac{f_{max} + f_{min}}{2}$$

Finally fraction tuning range is given by

$$Fractional\ Tuning\ Range = \frac{f_{max} - f_{min}}{f_0}$$

By above equations it's clear that by varying voltage of voltage dependent capacitor value help to compute C_{max}andC_{min}value of capacitor. This values help to compute tuning range of an LC oscillator. There are two types of varactor one is PN junction diode and the other is MOS cap varactor. This MOS varactor is used in two regions for variable capacitance first inversion and second is accumulation. The accumulation mode MOS varactor is not used because lack of suitable device model for that because of this reason in this thesis inversion mode MOS varactor used for VCO topology.

c) Power Dissipation: Today many wireless devices are required long life of battery which means that have low power consumption. But for VCO designer it's difficult to obtain low power consumption and low phase noise simultaneously. This because of tank voltage amplitude is proportional to current flowing. It means that there is trade-off exist between phase noise and power consumption.

In this paper, cross coupled differential topology is used. In this cross coupled differential topology as tank voltage changes the direction of current flow through tank reverse.The differential pair can be modeled as a current source switching between $I_{total}$and $-I_{total}$(which can also commonly refer as I_{baise}) in parallel with an RLC tank. The tank amplitude can be approximated as

$$V_{tank} \approx I_{total} \cdot R_{eq}$$

II. LITERATURE SURVEY

Nabil Boughanmi, et.al [1] proposed a high quality, low noise fully integrated Q-VCO in 0.35um CMOS technology. This Q-VCO phase noise is directly connected to the quality factor of the LC resonant circuit, which is mainly depending on quality factor of inductor. In their design they obtain high Q factors over 80 at 2.9 GHz. This Q-VCO exhibits lower phase noise performance for a given power dissipation. From a carrier at 2.9 GHz, dissipating 2.4 mA under a 2.5 V power supply and 1V tuning voltage, simulated phase noise results are -1.36 dBc / Hz at an offset of 100 kHz And -22 dBc / Hz at an offset of 100 MHz.

Albert Jerng, and Charles G. Sodini [2] present a impact of device type and sizing on phase noise mechanism for cross coupled differential topology. In their paper they show conversion of bias noise into phase noise through MOS switching transistor. They show minimization this phase noise through MOS device sizing rather than through filtering. In their paper they compare implementation of two cross coupled differential topology using NMOS and PMOS.

They finally concluded that PMOS based cross coupled differential topology has better phase noise performance in $1/f^2$ region and by reducing size of MOS switching transistor phase noise can be improve in $1/f^3$ region.

Ali Fard and PietroAndreani [3] presented Quadrature CMOS LC VCO with a wide frequency range of 3.6 GHz-5.6 GHz designed for multi standard front-end in 0.18um CMOS process. In this paper they compare this topology with double cross coupled topology and conventional QVCO structure. In their Experimental results on the QVCO show a phase noise level of-127.5 dBc/Hz at 3 MHz offset from a 5.6 GHz carrier while dissipating 8 mA of current, resulting in a figure of merit of181.3 dBc/Hz.

Mohd.ShahrulAmran et.al [3] demonstrated design of a 5 GHz differential cross-coupled LC oscillator is designed with Silterra's standard 8-layermetal 130 nm RF CMOS technology. The oscillator uses one copper inductor, two metal finger capacitors, two RF NMOS and two RF PMOS as its tank circuit. this proposed design, tank circuit has high quality factor inductor due to this it offered low phase noise, low power supply and temperature variation.

Lin Jia, et.al [4] presented a novel methodology for reducing phase noise in cross coupled LC tank VCO. In their paper they derive fundamental relation between phase noise and channel length of cross coupled MOS transistors is derived. Using this methodology they design 2GHz LC tank VCO by 0.18um CMOS technology. They obtain phase noise is -103.3 dBc/Hz at 100 kHz offset frequency and -118.9 dBc/Hz at 600 kHz offset with low-power consumption around 3.15 mW.

R. Saeidi, et.al [5] presented an analysis of phase noise differential cross coupled LC oscillator and a single-ended Colpitts oscillator were presented. In their paper they concluded that a single-ended Colpitts oscillator has better phase noise performance but consume more power compare to differential cross coupled LC oscillator.

Han-il Lee et.al [6] proposed extremely low power fully integrated CMOS cross coupled differential topology in a commercial 0.18 µm CMOS process.in design of LC tank they used high quality factor, low cost aluminum inductor and NMOS varactor. They measured phase noise is -111dBc/Hz at 1MHz offset from a 1.87 GHz carrier when the VCO core consumes only a 0.5 mW power from 0.9 V supply. They obtain tuning range of 1.86GHz ~ 2.01GHz for control voltage of 0V~1.4V.

Ali Fad et.al [7] demonstrated a comparative study of CMOS LC VCO Topologies in standard 0.35um CMOS technology for Wide-Band Multi-Standard Transceivers. In their study, they simulate both cross coupled differential and CMOS cross coupled differential topology and obtain result.The comparison shows that both circuits are applicable for multistandard transceivers. The complementary VCO shows 50% lower power dissipation with lower phase noise levels. Asa disadvantage, the circuit is suffering from larger parasitics and shows 500 MHz lower maximum operating frequency when compared to the NMOS structure. Although the NMOS topology consumes more current but by reducing the supply voltage the power dissipation significantly reduces due to this reason this topology more attractive for realization in digital technologies with lower supply voltages.

Jie Long and Robert J. Weber[8]proposed full integrated cross coupled differential topology in standard 0.18um single poly,6-metal mixed signal CMOS process. In this proposed topology they used NMOS varactor capacitance along with on chip spiral inductor to from LC Tank. They obtain 7% tuning range using NMOS varactor, power dissipation of 2.2mw and phase noise -122.1 dBc/Hz at a 1MHz offset for 2.4GHz.

III. DESIGN

The CMOS LC VCO circuit(Figure 3.1) is designed by using S-edit from Tanner EDA. The design CMOS LC VCO is simulated using in 65nm CMOS process. This section briefly discusses the simulated transient response and amplitude, tuning range and power consumption of the cross coupled differential LC-VCO designs. The focus is targeted on the measurement of parameters for CMOS LC VCO design.

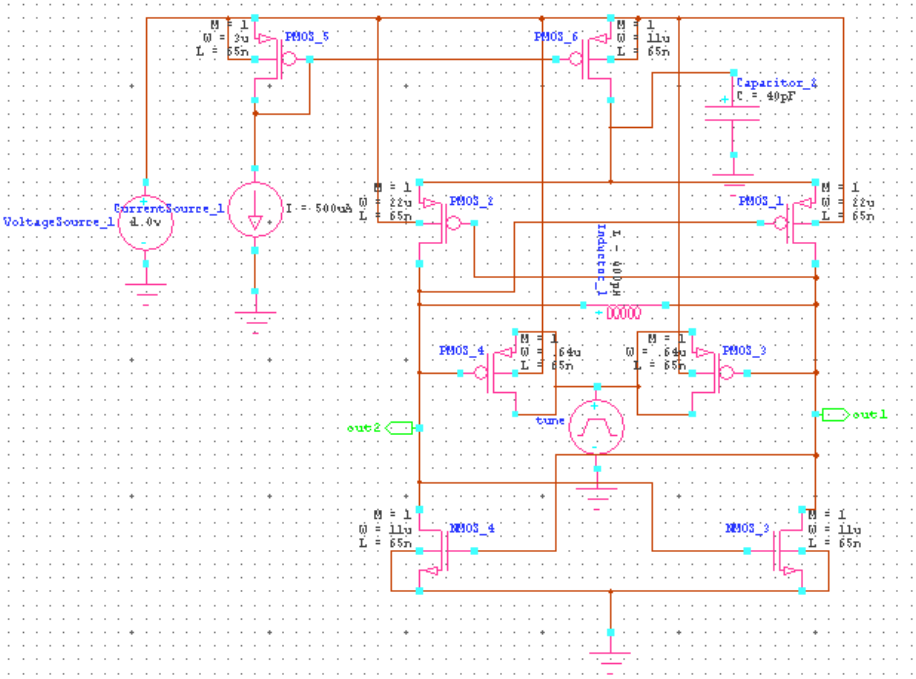

Fig.3.1 Schematic of LC VCO

3.1 Measurement of frequency

The frequency of CMOS LC VCO design can be calculated by transient response as show in Fig. 3.2. For frequency calculation, time period (dx) is directly read by oscillation as show in Fig. 3.2 which is equal to 34.4 ps at 1.0V. The relation between frequency and time is given below

$$F = \frac{1}{T}$$

In the above expression T is time period of oscillation. The time period of oscillation T is equal to dx. Substituting the value of time in above equation frequency comes out to be,

$$F = \frac{1}{34.4\ ps}$$

$$F = 29\ GHz$$

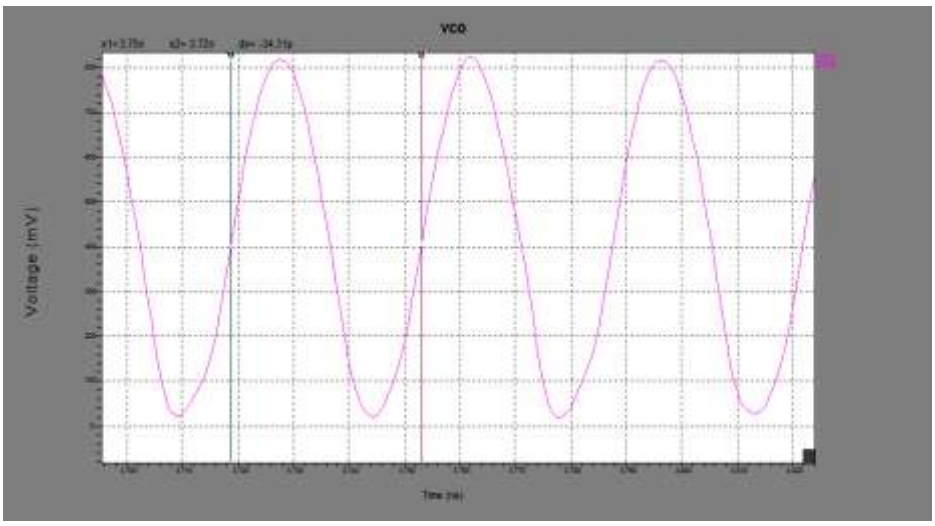

Fig. 3.2 Transient Response of LC VCO.

3.2Measurement of tuning range

The fractional tuning range of LC VCO design can be calculated by plotting graph between control voltages and frequencies as show in Fig.3.3 by transient analysis.

$$Fractional\ Tuning\ Range = \frac{f_{max} - f_{min}}{f_0} \times 100$$

By the graph is clear that f_{max}andf_{min} is 32.5 GHz and 27 GHz where f_0 is 29 GHz so fractional tuning range can be given by

$$Fractional\ Tuning\ Range = \frac{(32.5 - 27)GHz}{29\ GHz} \times 100$$

$$Fractional\ Tuning\ Range = 19\ \%$$

$$K_{VCO} = 2\pi \frac{(32.5 - 27)}{(1.0 - 0.0)}$$

$$K_{VCO} = 34.54 \frac{rad}{s} / voltage$$

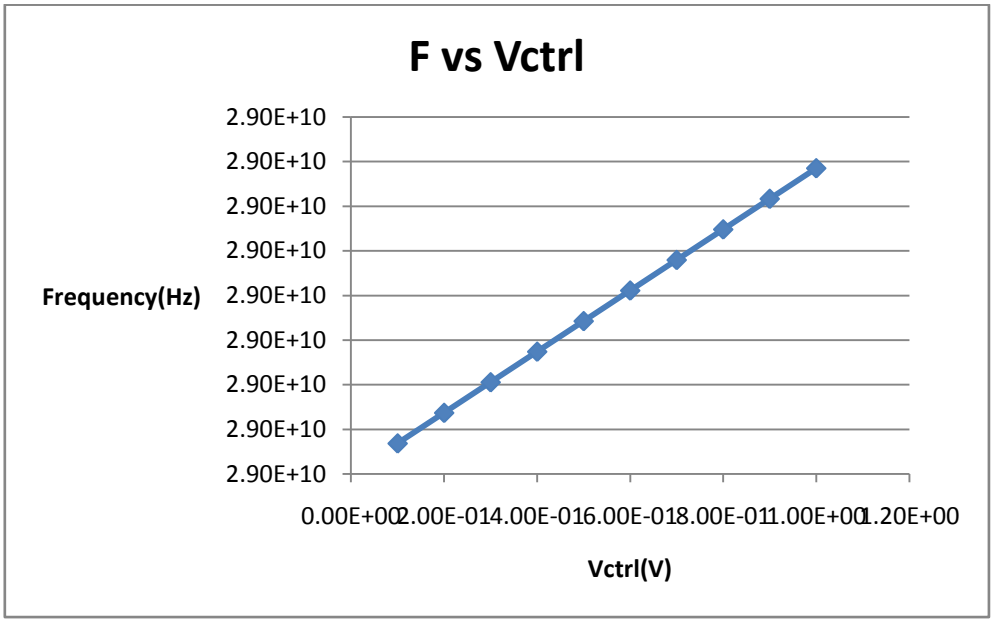

Fig.3.3 Relationship between voltage & frequency in VCO.

3.3 Power Consumption

The power consumption of VCO can be calculated by formula given below

$$\max d.c.\ \text{power dissipation} = V_{supply}\ I_{bias}$$

It gives total power consumed by the integrated parts in the circuit. The power consumed by this VCO is 500 uW according to formula.

IV. DESIGN

4.1 Tabulation of Parameters extracted

CMOS LC VCO design has very low power consumption. The low value of power is obtained due to implementation of cross coupled pair of PMOS transistor in design of LC VCO. This design of CMOS LC VCO has very optimized tuning range. The two PMOS are connected back to back and biased in inversion mode in design. In last area is computed using L-edit of tanner EDA. The results are summarized in Table 4.1.

Table 4.1

Results of CMOS LC VCO.

S.No.	Parameter	Simulation result
1.	Technology	65nm
2.	Power Consumption(uW)	500
3.	Frequency(GHz)	27-32.5
4.	Tuning Voltage(V)	0.0-1.0
5.	Tuning Range (%)	19

4.2 Phase Noise Contribution

The major contributors to the phase noise are listed in Table 4.2.

Table 4.2

Simulated Phase Noise Contribution @ f_o=29 GHz.

Device	Noise type	Noise contribution (V^2/Hz)	
		[9]	This work
Mp1,2	Flicker Noise	$1.88x10^{-8}$	$88x10^{-18}$
Mn1,2	Channel Noise	$4x10^{-9}$	$1.48x10^{-18}$
Mn1,2	Flicker Noise	$5.6x10^{-10}$	$18.67x10^{-15}$

4.3 Comparative study of results

Table 4.3

Comparison of CMOS LC VCO.

S.No.	Parameter	Ref. [1]	Ref. [3]	Ref. [4]	Ref. [5]	Ref. [7]	Ref. [9]	This work
1.	**Technology (nm)**	180	180	180	180	65	90	65
2.	**Supply Voltage (V)**	1.5	0.9	-	1.8	1.2	1.5	1.0
3.	**Power Consumption (mW)**	1.9	0.5	3.15	53.2	3.4	3.1	0.005
4.	**Frequency (GHz)**	2.28-2.59	1.86-2.01	1.9-2.2	1.8	0.75-1.5	27-32.5	27-32.5
5.	**Tuning Voltage(V)**	0-1.5	-	0-2.5	-	-	0.0-1.6	1.0-0.0
6.	**Tuning Rang*(GHz)**	0.31	0.15	0.3	-	0.75	5.5	5.5

V.CONCLUSION

A CMOS LC VCO is designed in 65nm CMOS process for high frequency application. This design is simulated on S-edit of Tanner EDA tool. In this design PMOS cross coupled pair transistor is implemented to reduce the up conversion of flicker noise in design. This PMOS cross coupled pair also help to reduce power consumption of circuit. In this design two P-type MOS varactor implemented to obtain good tuning range at low supply voltage. These two PMOS varactor provide a strong capacitance variation within few hundred of millivolts. The measured tuning range is from 27 GHz to 32.5 GHz with control voltage from 0.0 to 1.0V. This design has a very low power consumption of 500 uW. From previous section, it can been observed that phase noise contribution by mosfet's is very less as compared to the previous work.

REFERENCES

[1] Nabil Boughanmi,Dalenda ben issa, AbdennaceurkachouriandMounirsamet"High Q-VCO with Low phase noise for Communications applications",*in the International, Design and Test of Integrated Systems in Nanoscale Technology*, Conference, pp. 370- 373, 2007.

[2] Albert Jerng and Charles G. Sodini, "The Impact of Device Type and Sizing on Phase Noise Mechanisms",*IEEE journal Of Solid State Circuits*, Vol. 40, February 2005.

[3] Ali Fard and PietroAndreani, "**A** Low-Phase-Noise Wide-Band CMOS Quadrature VCO for Multi-Standard RF Front-Ends" in *Radio Frequency integrated Circuits (RFIC) Symposium*,pp. 539 – 542, June 2005.

[4] Mohd. ShahrulAmran, Queennie Lim SuanImm and Albert Victor Kordeschl, "Design of a 130nm CMOS Differential Cross-coupled 5 GHz LC Oscillator", *in proceeding of Asia-Pacific on applied electromagnatics*, pp.20-21, December 2005.

[5] Lin Jia, KiatSeng Yeo and ManhAnh Do, "A Novel Methodology for the Design of LC Tank VCO with Low Phase Noise", *in IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1, pp 376-379, 23-26 May 2005.

[6] R. Saeidi, N. Masoumi, F. Kalantari and M. S. Oskooei,"Analyzing of Phase Noise in CMOS LC Oscillators" *in the 17th International Conference on Microelectronics (ICM)*, pp. 330-337, Dec. 2005.

[7] Han-il Lee, Tae-young Choi, SaeedMohammadi and Linda P.B. Katehi, "An Extremely Low Power 2 GHz CMOS LC VCO for Wireless Communication Applications", *The European Conference on Wireless Technology*, pp. 31-34, Oct. 2005.

[8] Ali Fad, Tord Johnson, Martin Linder and Denny Biberg "A Comparative Study of CMOS LC VCO Topologies for Wide-Band Multi-Standard Transceivers",*The47thIEEE International Midwest Symposium on Circuits and Systems*, pp. 17-20 July 2004.

[9] Junyi Sun, ChirnChye Boon, Xi Zhu, Xiang Yi, KhannaDevrishi, and FanyiMeng,"A Low-Power Low-Phase-Noise VCO WithSelf-Adjusted Active Resistor" ,*IEEE Microwave and Wireless Components Letters*, 2016.

