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FPGA Implementation of Multi-notch Comb Filter

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***Abstract*—** A comb filter in HDL is implemented which will notch the desired multiple of sampling frequency. The implementation of the filter will be done using infinite impulse response (IIR) scheme of designing digital filters. The input will be sampled using an ADC and the filtered output will be obtained from DAC. The filter will reside in a FPGA.

***Index Terms*—** Comb Filter, FPGA, ADC, DAC, Sampling Frequency.

I. Introduction

The electrocardiogram obtained during the tests is contaminated by disturbances such as supply-line frequency components and base-line wander. We need to remove these disturbances in first step to process the ECG not only automatically but also for visual diagnosis. This task is achieved by using the comb filter whose frequency response is periodic in nature with stop band notches at 0Hz to remove base-line wander. Also the stop band notches are at 50Hz and higher harmonics to remove power-line disturbances [1] [2].

A comb filter can be designed using infinite impulse response technique (IIR) and finite impulse response technique (FIR). If the fundamental frequency of the harmonics is known than a fixed comb filter can be used and if unknown or time varying than adaptive comb filter will be applicable [3].

In upcoming sections we will describe the technique used in HDL implementation of comb filter using the IIR scheme.

II. Theory

To introduce a notch at a particular frequency we introduce a pair of complex conjugate zeros on the unit circle. The bandwidth of such notches is large. In order to reduce the bandwidth of notches we introduce a pair of complex conjugate poles very near to the unit circle. These poles introduce resonance in the vicinity of the notches, and reduce the bandwidth.

The transfer function for the multi-notch/Comb filter is given by,

$$H(z) = \frac{1 - z^{-k}}{1 - R^k z^{-k}}$$

Where,

$$k = \frac{2\pi}{Harmonics\ of\ sampling\ frequency\ where\ we\ desire\ to\ have\ notches}$$

$$R < 1 = magnitude\ of\ pole$$

On simplifying the transfer function we get,

$$\frac{Y(z)}{X(z)} = \frac{1 - z^{-k}}{1 - R^k z^{-k}}$$

$$Y(z) - R^k z^{-k} Y(z) = X(z) - z^{-k} X(z)$$

$$Y(z) = X(z) - z^{-k} X(z) + R^k z^{-k} Y(z)$$

In time domain the output of comb filter is given by,

$$y(n) = x(n) - x(n-k) + R^k y(n-k)$$

Fig.1 and fig.2 shows the magnitude and phase response of the comb filter for sampling frequency of 10 KHz. The filter notches the harmonics of 0.2π (0.1×5 KHz).

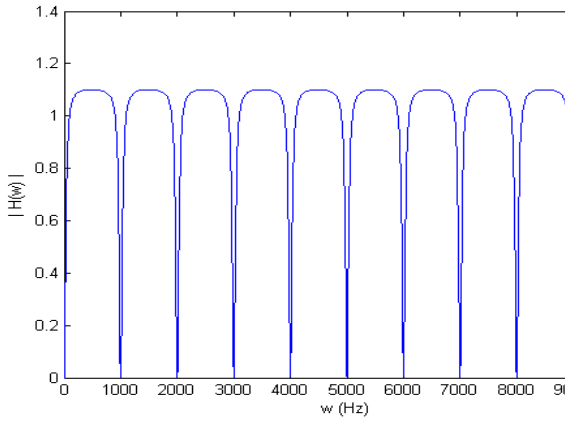


Fig.1 Magnitude Response

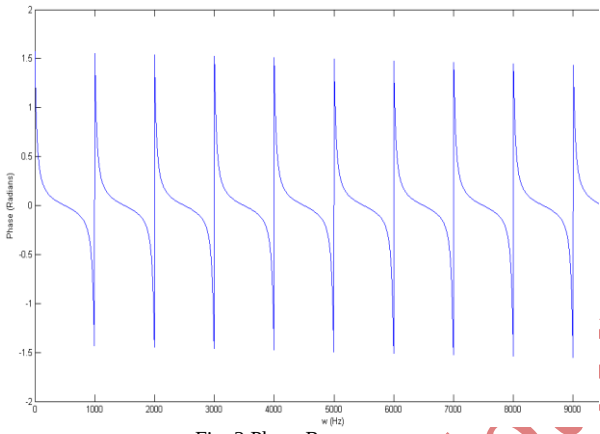


Fig. 2 Phase Response

III. Design Specifications

Following are the design specifications used to calculate various parameters of the filter,

1. Sampling frequency: 128 KHz.
2. Harmonics: 1 KHz, 2 KHz, 3 KHz... 64 KHz.
3. R = 0.998

Following parameters are derived from above specifications,

1. Harmonics: 0.0156π.
2. k = 128
3. Transfer Function: $H(z) = \frac{1-z^{-128}}{1-R^{128}z^{-128}}$
4. $Y(z) = X(z) - z^{-128}X(z) + 0.998^{128}z^{-128}Y(z)$

IV. Implementaion

A. *System Block Diagram*

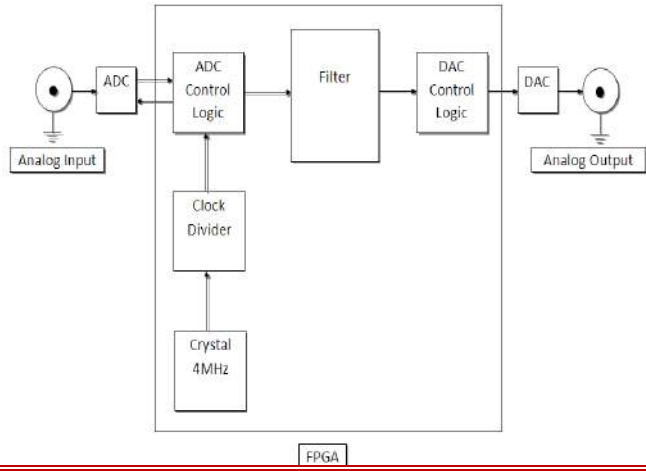


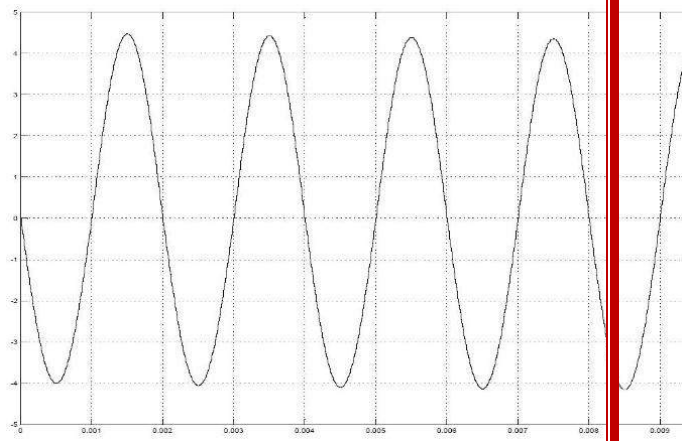
Fig.3. System Block Diagram

The block diagram has three major blocks viz. ADC, FPGA, DAC. The ADC will convert the analog input signal into digital data bits. A 12 bit ADC AD7891 with sampling frequency up to 500KSPS is used for this purpose.

The FPGA will have the HDL implementation of the digital comb filter. The output of ADC will be given as input to this digital filter. A Xilinx Spartan 3 series FPGA is used for this purpose. The HDL implementation, along with the digital filter, will also implement the interface of ADC and DAC with the FPGA. This interface will include the control signals to ADC and DAC and required data manipulation.

The output of the filter in the FPGA will be then given as input to a DAC. The DAC will convert the digital bits output back into analog form. A 12 bit DAC AD7541 is used for this purpose.

V. Results



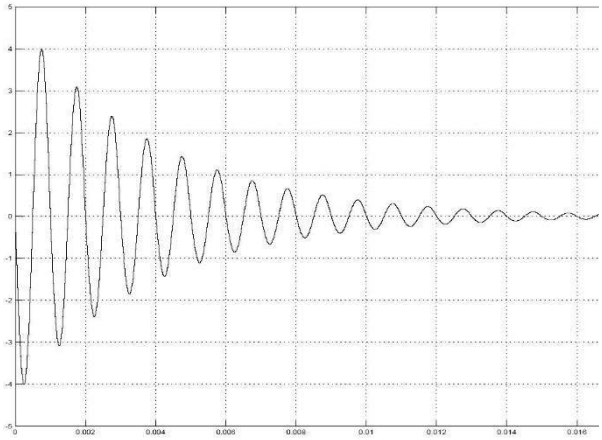


Fig.4 Output Waveform at 500 Hz & 1 KHz respectively

VI. CONCLUSION

It can be seen from the table above that the resources used in our design are much larger than that estimated by the 'Xilinx Resource Estimator". But, as a matter of fact that our code also consists of ADC and DAC, whereas the estimated results are only for the filter designed using system generator and it doesn't include ADC and DAC.
Hence, in the light of above mentioned argument we conclude that our design is better and holds the requirements of area, speed, and power consumption.

Resources	Our Design	Xilinx Resource Estimator
Slices	198	157
FFs	80	192
BRAMs	0	0
LUTs	343	310
IOBs	35	24
Emb. Mults	2	1
TBUFs	0	0

REFERENCES

[1] J.A. Van Alste and T.S. Schilder, "Removal of Base-Line Wander and Power-Line Interference from the ECG by an Efficient FIR Filter with a Reduced Number of Taps" in *IEEE Transaction on Biomedical Engineering*, vol. BME-32, No. 12, December 1985.
[2] Soo-Chang Pei and Chien-Chien Tseng,"A Comb Filter Design Using Fractional-Sample Delay" in IEEE Transaction on Circuits and Systems – II: Analog and Digital Signal Processing, Vol. 45, No. 6, June 1998.
[3] Pavel Zahradnik and Miroslav Vlcek, " Analytical Design for Optimal Equiripple Comb FIR Filters", in IEEE Transacttions on Circuits & Systems-II:Express Briefs, Vol. 52, No. 2, Feburary 2005.
[4] Digital Signal Processing, John G Proakis and Dimitris G Manolakis.
[5] DSP FPGA Workbook.
[6] Mechatronics DSP Kit Manual.
[7] Datasheet AD7891 : LC2 CMOS 8-Channel 12-bit High Speed Data Acquisition System.
[8] Datasheet AD7541 : 12-bit Monolithic Multiplying DAC.