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# Design and Verification of MSIC Test Pattern Generator

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## ABSTRACT

*Improvement in quality and reliability are required for digital circuits as their complexity and density increases. Validation of VLSI circuits becomes more difficult with higher test cost. Built-In-Self-Test (BIST) techniques can effectively reduce complexity of VLSI testing, by the introduction of on-chip test hardware into the Circuit Under Test (CUT). In BIST architectures, the Test Pattern Generator (TPG) uses Linear Feedback Shift Register (LFSR) which generates pseudo random patterns that increases the switching activity of test patterns. The proposed test pattern generator generates a multiple single input change (MSIC) vector which increases the accuracy of test response. The Single Input Change (SIC) vector generator uses a reconfigurable Johnson counter to generate minimum transition sequences. The proposed TPG can be used in both test-per-clock and test-per-scan schemes. The verification of the circ test is done using a reversible technique and a Look-Up-Table (LUT) method. The proposed system is simulated using Xilinx13.2.*

**Keywords: BIST, CUT, LFSR, MSIC, Reconfigurable Johnson Counter.**

## 1. INTRODUCTION

To eliminate the various defects caused by the manufacturing process, System on Chip (SoC) circuits depends on testing. Testing is the indigenous phase which attribute towards the successful implementation of any device. Importance of testing in Integrated Circuit is to improve the quality in chip functionality that is applicable for both commercially and privately produced products.

In Today's IC, as designs become more complicated Built In Self Test (BIST) has become progressively important. In order to test any circuit or device we require separate testing technique which should be done automatically. A BIST is used for this purpose. Built in self test techniques can effectively reduce the difficulty and complexity of VLSI testing. Thus BIST has become one of the major test techniques for today's large scale and high speed designs.

BIST is a Design For Test (DFT) methodology that aims at detecting faulty components in a system by introducing the test logic into the chip [1]. BIST is better known for its numerous advantages such as at-speed testing and reduced need for expensive external Automatic Test Equipment (ATE). The steps in a typical BIST approach are:

1) On-chip generation of test pattern.
2) Application of the test patterns to the circuit under test.
3) Analysis of circuit under test responses with on-chip output response analyzer (ORA)
4) Making decision whether the chip is faulty or not.

An efficient Test Pattern Generator (TPG) design is related to on-chip test pattern generation and it is an important subject in built in self test schemes. The basic BIST architecture shown in Figure1 consists of a test pattern generator (TPG), circuit under test (CUT) and an output response analyzer (ORA) also called as Output Data Analyzer (ODA) [2]. Test patterns for the circuit under test are generated by the test pattern generator. In conventional BIST architectures, the Linear Feedback Shift Register (LFSR) is commonly used in the test pattern generators due to simplicity and effectiveness of the LFSRs. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the circuit under test [3], which can cause excessive power dissipation in the circuit under test. They also can damage the circuit and reduce the product yield and lifetime of



CUT [4], [5]. The random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among the adjacent bits within each pattern. Therefore it is necessary that the patterns generated by the test pattern generator must have only minimum transitions. A typical response analyzer is a comparator that compact stored responses of all possible inputs and analyzes the test responses to determine correctness of the circuit under test.

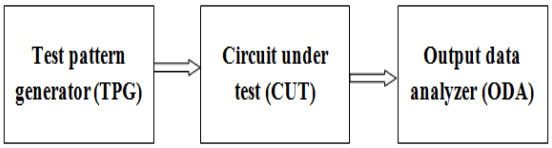



**Figure. 1: Basic BIST Architecture.**

For today's system on chips design and test, power dissipation is a challenging problem. The power dissipation in CMOS technology is either static or dynamic. The dynamic power which is consumed when the circuit nodes switch from 0 to 1 is the dominant factor in the power dissipation. The power is consumed during switching, due to the short circuit current flow and the charging of load capacitances. In general, power dissipation of a system in test mode is more than in normal mode [1]. This is because; between consecutive vectors applied during the circuit's normal mode of operation there exists a significant correlation, whereas this may not be necessarily true for the applied test vectors in the test mode.

Low correlation that exists between the consecutive test vectors increases switching activity and eventually power dissipation in the circuit during the test mode. The same happens when applying low correlated patterns to scan chains. The increasing switching activity in scan chain results in increasing power consumption in scan chain and its combinational block. The increase in power during test mode [2] is due to the following reasons:

1) High switching activity due to nature of the test patterns.
2) Parallel activation of internal cores during test.
3) Consumption of power by extra design for test circuitry.
4) Low correlation that exists among test vectors.

Several problems [1] are caused due to this extra power such as formation of hot spots, instantaneous power surge that causes circuit damage, difficulty in performance verification and reduction of the product yield and lifetime. By controlling the switching activity in the test patterns, the power dissipation during testing can be reduced. Hence the important aspect is to optimize power during testing [6]. Power reduction using the switching activity doesn't degrade the performance of the circuit rather it increases the accuracy. Several faults due to increased switching activity of the test patterns such as stuck at faults, bridging faults, etc. can be reduced and thus the accuracy of the test response can be improved.

The TPG can be modified by adding a Johnson counter (or twisted ring counter) to the LFSR. This technique decreases the switching activity of the circuit under test and increases the fault coverage and generates the Multiple Single Input Change (MSIC) vectors for the test pattern generator. MSIC test pattern generator generates a minimum transition sequence that is; it generates test patterns with change only in single bit position. The switching activity in the circuit under test and the scan chains and, eventually, their power consumption are reduced by increasing the correlation between patterns and also within each pattern in the generated scan chain.

The rest of this paper is organized as follows. In Section 2, the MSIC-TPG scheme is presented. The verification of new MSIC test patterns in the circuit under test is described in Section 3. In Section 4, the simulation results of both test per clock and test per scan are provided to demonstrate the performance of the MSIC-TPGs. Two techniques for the verification of the circuit under test are also included in this chapter. Conclusions and the future scopes of this paper are given in Section 5.

## 2. MSIC TEST PATTERN GENERATOR

Multiple Single Input Change (MSIC) is a test pattern generator (TPG) method that can change a Single Input Change (SIC) vector to exclusive low transition vectors for multiple scan chains [7],[9]. The first step in this process is to decompress the SIC vector to its multiple code words and the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The MSIC TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

### 2.1 Test Pattern Generation Method

Consider *m* primary inputs (PIs) and *M* scan chains in a full scan design, and each scan chain has *l* scan cells. Figure 2 shows the symbolic representation for one generated pattern.

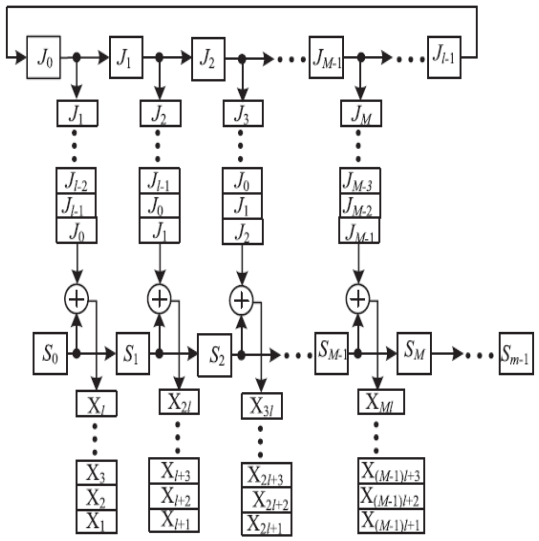


**Figure 2: Symbolic representation of an MSIC pattern[7].**

The generated vector of an *m*-bit LFSR with the primitive polynomial can be expressed as $S(t) = S_0(t)S_1(t)S_2(t), \ldots, S_{m-1}(t)$ (hereinafter referred to as the seed), and the vector generated by an *l*-bit Johnson counter can be expressed as $J(t) = J_0(t)J_1(t)J_2(t), \ldots, J_{l-1}(t)$. In the first clock cycle, $J = J_0\ J_1\ J_2, \ldots, J_{l-1}$ will bit-XOR with $S = S_0S_1S_2, \ldots, S_{M-1}$, and the results $X_1X_{l+1}X_{2l+1}, \ldots, X_{(M-1)l+1}$ will be shifted into *M* scan chains, respectively. In the second clock cycle, $J = J_0\ J_1\ J_2, \ldots, J_{l-1}$ will be circularly shifted as $J = J_{l-1}\ J_0\ J_1, \ldots, J_{l-2}$, which will also bit-XOR with the seed $S = S_0S_1S_2, \ldots, S_{M-1}$. The resulting $X_2X_{l+2}X_{2l+2}, \ldots, X_{(M-1)l+2}$ will be shifted into *M* scan chains, respectively. After *l* clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed $S_0S_1S_2, \ldots, S_{m-1}$ will be applied to *m* PIs.

Since the circular Johnson counter can generate *l* unique Johnson codewords through circular shifting a Johnson vector, the XOR gates and circular Johnson counter actually constitute a linear sequential decompressor.

There are two kinds of SIC generators based on the different scenarios of scan length, to generate Johnson vectors and Johnson codewords, that is; the reconfigurable Johnson counter and the scalable SIC counter. For a short scan length, a reconfigurable Johnson counter is developed as shown in Figure 3 to generate an SIC sequence in time domain. An SIC counter named the "scalable SIC counter" is developed when the maximal scan chain length *l* is much larger than the scan chain number M. The SIC counter consist of subtractor, adder, chain of D flipflops and chain of muxes.

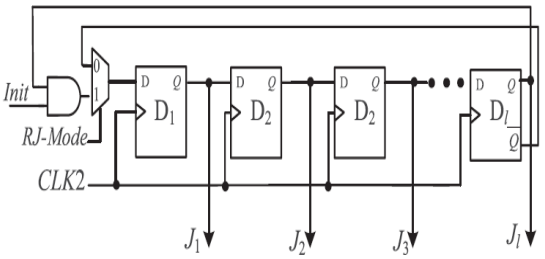


**Figure 3: Reconfigurable Johnson counter[7].**

Reconfigurable Johnson Counter is preferably used when the scan length is less. The reconfigurable Johnson counter consists of a mux and an AND gate to make it operate in three different modes. The control signals for the reconfigurable Johnson counter are Init and RJ_Mode. The reconfigurable Johnson counter has three modes of operation:

1) *Initialization*: When Init is set to logic 0 and RJ_Mode is set to 1, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than *l* times.

2) *Circular shift register mode*: When Init and RJ_Mode are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 *l* times.

3) *Normal mode*: The reconfigurable Johnson counter will generate 2*l* unique SIC vectors by clocking CLK2 2*l* times when RJ_Mode is set to logic 0

## 2.2 MSIC-TPG for Test per Clock schemes

The MSIC-TPG for test-per-clock schemes is illustrated in Figure 4. The circuit under test's primary inputs $X_1 - X_{mn}$ are arranged as an n × m SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed generator output and an output of the Johnson counter. The outputs of the XOR gates are applied to the circuit under test's primary inputs. A seed generator is an m-stage conventional LFSR, and operates at low frequency CLK1. The test procedure for the test per clock scheme is as follows:

1) The seed generator generates a new seed by clocking CLK1 one time.
2) The Johnson counter generates a new vector by clocking CLK2 one time.
3) Repeat 2 until 2*l* Johnson vectors are generated.
4) Repeat above steps until the expected fault coverage or test length is achieved.



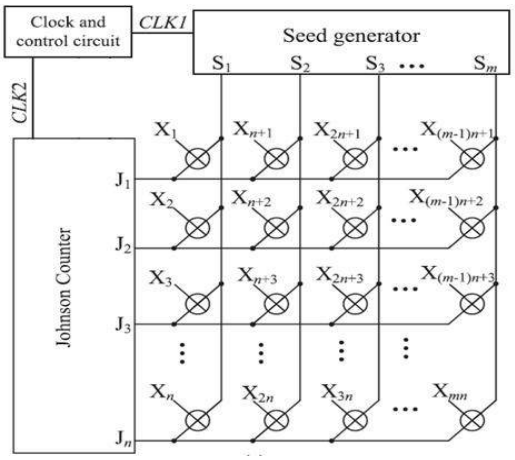



**Figure 4: MSIC-TPGs for test-per-clock scheme**

## 2.3 MSIC-TPG for Test per Scan schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Figure 5. The inputs of the XOR gates come from the Johnson counter and the seed generator and their outputs are applied to M scan chains, respectively. The output of the XOR gate is applied to the circuit under test's primary inputs, respectively. The test procedure for the test per scan scheme is as follows:

1) The seed circuit generates a new seed by clocking CLK1 one time.
2) RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3) After a new Johnson vector is generated, Init and RJ_Mode are set to 1. Now the reconfigurable Johnson counter operates as a circular shift register, and generates *l* codewords by clocking CLK2 *l* times. Then, a capture operation is inserted.
4) Repeat 2–3 until 2*l* Johnson vectors are generated.
5) Repeat the above steps until the expected fault coverage or test length is achieved.

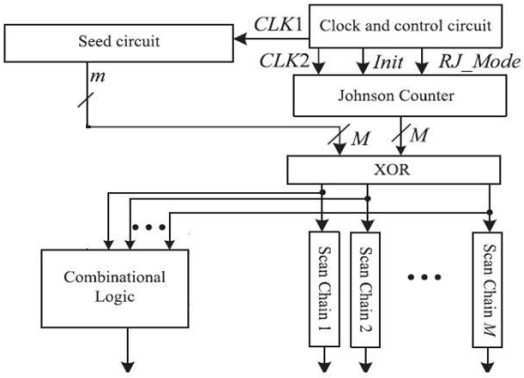



**Figure 5: MSIC-TPGs for test-per-scan scheme.**

The main objective of the test pattern generator designed to produce single input change vector is to reduce the switching activity. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency [8]. Finally, uniformly distributed patterns are desired to reduce the test length (number of patterns required to achieve a target fault coverage).

## 3. VERIFICATION OF MSIC TEST PATTERN GENERATOR

The correct test patterns generated by the test pattern generator, only produces the error free test responses. Therefore for testing the circuit under test, verified test patterns should be applied to the circuit under test. The verification of the circuit under test is done by checking the correctness of the test response of the CUT. This can be done in two ways. First is by using a reversible technique in the circuit under test. Another method is by using a Look Up Table (LUT). A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT.

### 3.1 Reversible Technique

The MSIC-TPG produces unique single input change patterns which are applied to the circuit under test. The test responses produced from the circuit under test are applied to the reversible logic circuit of the respective circuit under test. If the output from the reversible technique and the patterns applied to CUT are same, there is no error in the test response of the circuit. Thus we can minimize the error in the CUT by applying the MSIC patterns generated from the MSIC test pattern generator. Figure 6 gives the idea of reversible technique used in this work.

### 3.2 Look Up Table Method

Look up tables may be pre-calculated and stored in static program storage or stored in hardware for application specific platforms. To test the fault coverage of the test pattern generator a combinational circuit will be used as circuit under test and output response of the CUT is stored in Look Up Table (LUT) for error comparison. Test responses are obtained after applying the test patterns from the MSIC test pattern generator to the circuit under test. Based on the circuit, output values are stored in the LUT corresponding to the inputs. LUT method compares the test response of the circuit under test and the data stored in the look up table.

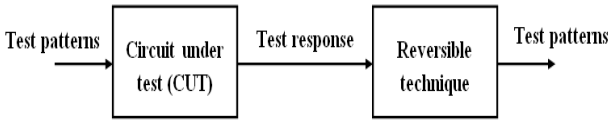


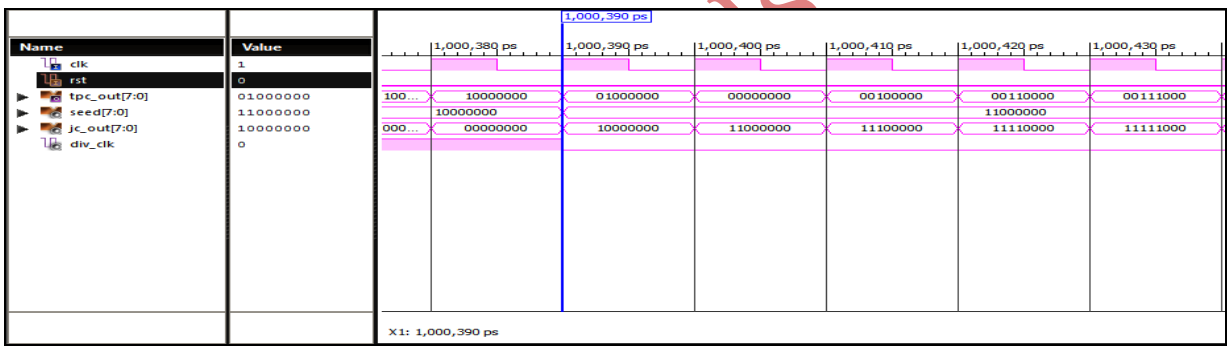

**Figure 6: Reversible technique**

## 4. RESULTS

The MSIC TPG based BIST is programmed on VHDL and this test pattern generator greatly simplifies the testing process. In this section all the simulation results of test pattern generation and verification of test patterns are shown. The performance simulations of MSIC TPG along with CUT testing are carried out with Xilinx 13.2.The simulated output for the proposed MSIC test pattern generator shown in Figure 7(a) and Figure 7(b). The verification of the circuit under test using reversible technique and LUT method is shown in Figure 7(c) and Figure 7(d) respectively.

## 5. CONCLUSION

This paper is based on low-power test pattern generation method. Simulation results showed that an MSIC sequence had the favorable features of minimum transitions, uniqueness and uniform distribution of patterns. A flexible test per scan and test per clock schemes can be developed with the combination of Reconfigurable Johnson counter. The MSIC sequence produced by the MSIC test pattern generator does not contain any repeated test patterns. Thus the proposed system improves the test efficiency and reduced the test time. This method also reduces the power consumption during testing mode with minimum number of switching activities between test patterns. After generating the MSIC patterns, the validation process is conducted on the combinational logic circuit and the output is verified via two techniques, the reversible technique and the LUT technique. In future work, the two techniques for verification, the reversible technique and the look up table method can be implemented on FPGA and a comparison can be made between these two techniques in terms of area and delay.

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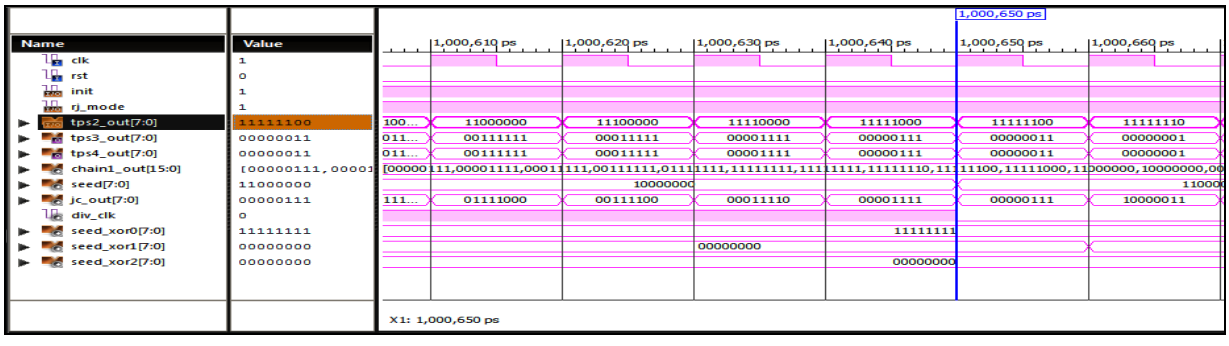


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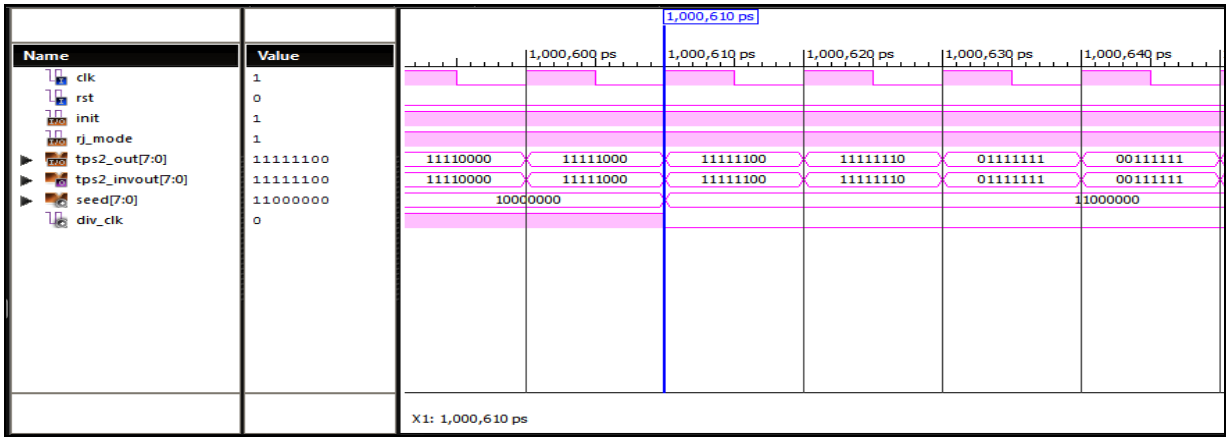


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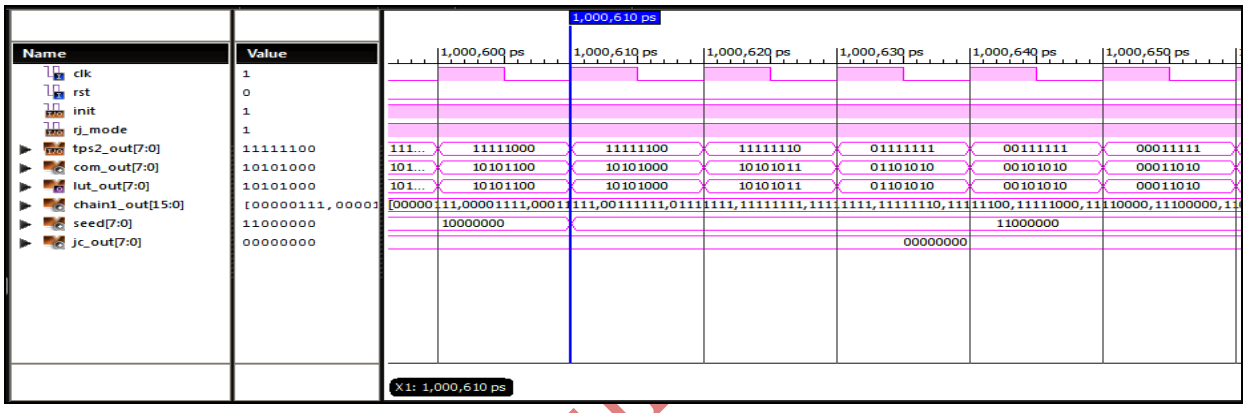


**(d)**

**Figure 7: Simulation result of (a) Test per clock (b) Test per scan (c) reversible technique (d) look up table method**

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