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# A HIGHLY MEMORY AND COMPUTATION EFFICIENT VLSI ARCHITECTURE FOR 2D DWT USING LIFTING SCHEME

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***Abstract:-*** In this paper, we propose a superior and memory-proficient pipeline engineering which plays out the one-level two-dimensional discrete wavelet change (2-D DWT) in the 5/3 and 9/7 channels. All in all, the interior memory size of 2-D design exceedingly relies on upon the pipeline registers of 1-D DWT.

In view of the lifting-based DWT calculation, the primitive information way is altered and an effective pipeline design is inferred to abbreviate the information way. In like manner, under the same number-crunching assets, the 1-D DWT pipeline design can work at a higher handling speed (up to 200MHz in .25um innovation) than other pipelined models with direct usage. The proposed 2-D DWT design is made out of two 1-D processors (segment and column processors). In light of the adjusted calculation, the line processor can incompletely execute every line savvy change with just two section prepared information. Consequently, the pipeline registers of 1-D engineering don't completely transform into the inward memory of 2-D DWT. For a NxM picture, just 3.5N inside memory is required for the 5/3 channel, and 5.5N is required for the 9/7 channel to play out the one-level 2-D DWT decay with the basic way of one multiplier delay (i.e. N and M show the stature and width of a picture). The pipeline information way is customary and practicable. At last, the proposed engineering actualizes the 5/3 and 9/7 channels by falling the three key parts.

Index Terms: lifting-based DWT, two-dimensional discrete wavelet transform, JPEG 2000.

## I. INTRODUCTION

The Discrete Wavelet Transform (DWT) assumes a noteworthy part in the fields of sign examination, PC vision, object acknowledgment, picture pressure and video pressure standard. The benefit of DWT over other customary changes is that it performs multi determination examination of signs with restriction both in time and recurrence as portrayed by Mallat [3]. At present, numerous VLSI models for the 2-D DWT have been proposed to meet the necessities of continuous preparing. The execution of DWT in common sense framework has issues. To start with, the multifaceted

nature of wavelet change is a few times higher than that of DCT.

Second, DWT needs additional memory for putting away the middle of the road computational results. Additionally, for ongoing picture pressure, DWT needs to handle monstrous measures of information at high speeds. The utilization of programming execution of DWT picture pressure gives adaptability to control however it may not meet planning requirements in specific applications. Equipment execution of DWT has useful impediments. To begin with, is that the high cost of equipment execution of multipliers Filter bank usage of DWT contains two FIR channels. It has generally been executed by convolution or the limited motivation reaction (FIR) channel bank structures. Such executions require both vast number of math calculations and capacity, which are not attractive for either fast or low power picture/video handling applications. Subsequently another methodology called the lifting plan based wavelet change was proposed taking into account a spatial development of the second era wavelet and an extremely adaptable plan for its factorization has been suggested. The lifting plan has numerous focal points over the past methodologies. Specifically, all the intriguing properties of wavelets, for example, bi-orthogonality and normality, are characterized by straight connections between the channel bank coefficients. As a result, it is simpler to outline wavelet channels. Dissimilar to convolutional wavelets, lifting plan does not rely on upon Fourier change of the wavelets. As a result, wavelets can be outlined on discretionary cross sections in spatial area. Since the lifting plan makes ideal utilization of likenesses between the high and low leave channels to speed behind the estimation of wavelet change, it has been



 

embraced in the picture pressure standard JPEG2000. The different structures contrast as far as required quantities of the multipliers, adders and registers, and in addition the measure of getting to outer memory, and prompts diminish effectively the equipment cost and power utilization of design. Inspite of enhancing the proficiency of existing models, the present prerequisite is to enhance the equipment usage and fit for taking care of various information streams for the count of 2D DWT.

## II. DISCRETE WAVELET TRANSFORM USING CONVOLUTION

The innate time-scale area attributes of the discrete wavelet changes (DWT) have set up as effective instrument for various applications, for example, signal investigation, signal pressure and numerical examination. This has driven various examination gatherings to create calculations and equipment structures to execute the DWT. Discrete wavelet change (DWT) is by and large progressively utilized for picture coding. This is because of the way that DWT bolsters highlights like dynamic picture transmission, simplicity of compacted picture control, locale of enthusiasm coding and so forth. The VLSI designs proposed in for equipment usage of DWT are fundamentally convolution-based. In the ordinary convolution strategy for DWT, a couple of Finite Impulse Response channels (FIR) is connected in parallel to infer high pass and low-pass channel coefficients pyramid calculation [3] can be utilized to speak to the wavelet coefficients of picture in a few spatial introductions. The designs are for the most part collapsed and can be extensively characterized into serial and parallel models. The design in [5] executes channel bank structure effectively utilizing digit serial pipelining. The engineering proposed in [1] utilizes polyphase decay and coefficient collapsing procedure for effective execution of discrete wavelet change. A general style in which DWT disintegrates the information picture is appeared beneath in Fig.1.

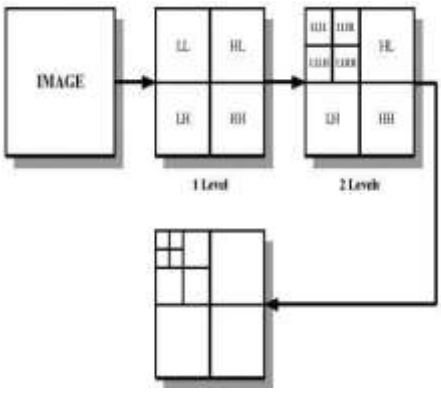


**Figure. 1 Three level decomposition of an image**

## III. LIFTING BASED DWT

The lifting plan is another strategy to build wavelet premise, which was initially presented by Swelden's. The lifting plan completely depends on the spatial space, has numerous focal points contrasted with channel bank structure, for example, lower zone, power utilization and computational many-sided quality. The lifting plan can be effortlessly actualized by equipment because of its essentially diminished calculations. Lifting has different points of interest, for example, "set up" calculation of the DWT, number to-whole number wavelet changes which are helpful for lossless coding. The lifting plan has been developed as an adaptable device reasonable for building the second era wavelets. It is made out of three fundamental operation stages: split, foresee and upgrade. Fig.3. demonstrates the lifting plan of the wavelet channel registering one measurement signal.The three basic stages in Lifting based DWT are:

Split step: where the sign is part into even and odd focuses, in light of the fact that the most extreme correlation between nearby pixels can be used for the following anticipate step. For every pair of given information tests x(n) split into even x(2n) and odd coefficients x(2n+1).

Predict step: The even examples are increased by the anticipate variable and afterward the outcomes are addedto the odd specimens to produce the point by point coefficients (dj).Detailed coefficients results in high pass separating.

**Update step**: multiplied by the update factors and then the The detailed coefficients computed by the predict step are results are added to the even samples to get the coarse coefficients (sj).The coarser coefficients gives low pass filtered output.

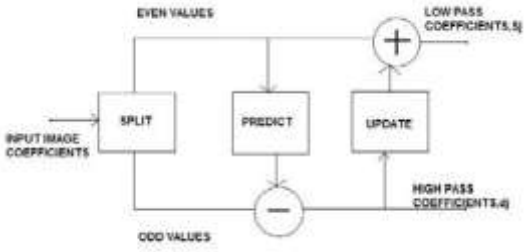


**Figure. 2 Block diagram of forward Lifting scheme**

## IV. TWO-DIMENSIONAL DISCRETE WAVELET TRANSFORM

The main challenges in the hardware architectures for 1-D DWT are the processing speed and the number of multipliers and adders while for 2-D DWT it is the memory issue that dominates the hardware cost and the

architectural complexity. A 2-D DWT is a separable transform where 1-D wavelet transform is taken along the rows and then a 1-D wavelet transform along the columns. The 2-D DWT operates by inserting array transposition between the two 1-D DWT.The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients. This process is repeated again with the columns, resulting in four sub-bands within the array defined by filter output.as in three-level decomposition. detailed data flow graph (DFG), which represents the calculations of one lifting step in the modified algorithm. The processor reads one input sample in each cycle, and then multiplies it by the corresponding coefficient in the following cycle. After each input datum is multiplied, the rest of the calculation only requires several addition operations.

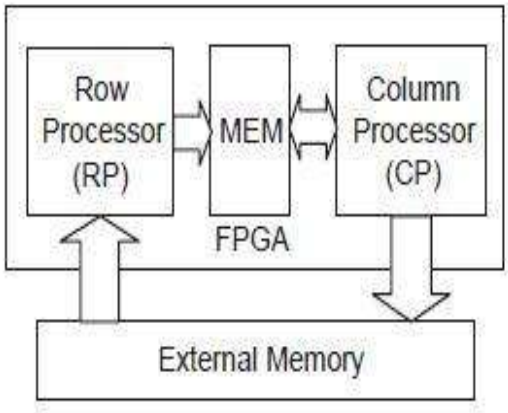


Figure 3. A Generic 2D DWT processor

The LL sub-band represents an approximation of the original image, the LL1 sub-band can be considered as a 2:1 sub-sampled version of the original image. The other three sub-bands HL1, LH1, and HH1 contain higher frequency detail information. This process is repeated for as many levels of decomposition as desired. The JPEG2000 standard specifies five levels of decomposition [21], although three are usually considered acceptable in hardware. In order to extend the 1-D filter to compute 2-D DWT in JPEG2000, two points have to be taken into account:
Firstly, the 1-D DWT generates the control signal memory to compute 2-D DWT and manages the internal memory access. Secondly, we need to store temporary results generated by 2-D column filter. The amount of the external memory access and the area occupied by the embedded internal buffer are considered the most critical issues for the implementation of 2D-DWT. As the cache is used to reduce the main memory access in the general processor architectures, in similar way, the internal buffer is used to reduce the external memory access for 2D-DWT. However, the internal buffer would occupy much area and power consumption.

## V. PROPOSED ARCHITECTURE

The column processor can be regarded as a 1-D DWT processor acting on the column-wise image data. The proposed column processor [2] is optimized in terms of the arithmetic cost and processing speed.

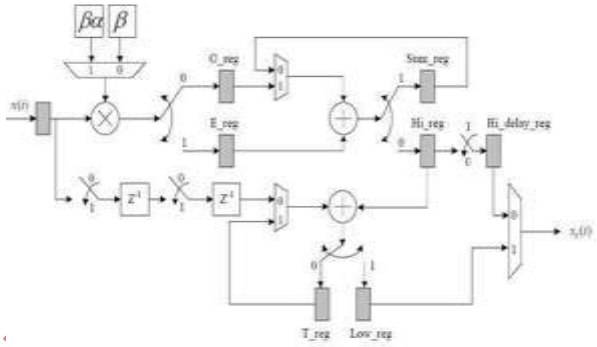

Figure 4.1: 1-D DWT architecture for column Processor

Fig. 4.2 plots the the timing diagram of the DFG in figure 4.2, shows that only one multiplier and two adders are needed at each clock cycle for the computations, and thecritical path between the pipeline registers is mainly limited by one multiplier delay.

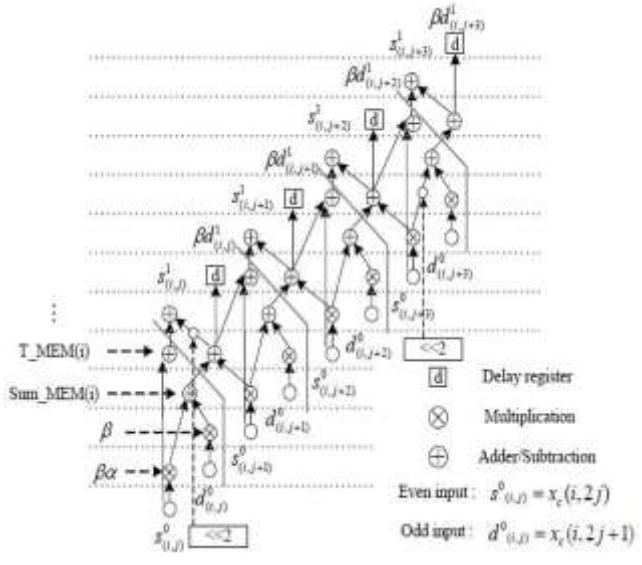


**Figure 4.2: The data path of the i-th column-wise transform**

The row-wise transform can be considered as the transpose of the column process and is easy to perform in principle. In the hardware implementation, to reduce the internal memory requirement, the column-processed data have to be executed as soon as possible. Moreover, the internal memory size of row processor highly depends on the pipeline registers of 1-D architecture. The trade-off between high speed and less memory is an important issue for the 2-D DWT architecture. Based on the modified algorithm, the column-processed data can be partially executed todecrease the internal memory size. Fig. 4.3 indicates the i-th row-wise data path of the modified DWT algorithms. Once two column processed data are collected, the i-th row-wise transform is then partially performed and the results are temporarily stored in the "Sum_MEM (i)" and "T_MEM (i)", where the index i is from 0 to N-1. That is, "Sum_MEM (i)" and "T_MEM (i)" are used to preserve the data path of each row transform and the data path is updated by the two new input data.

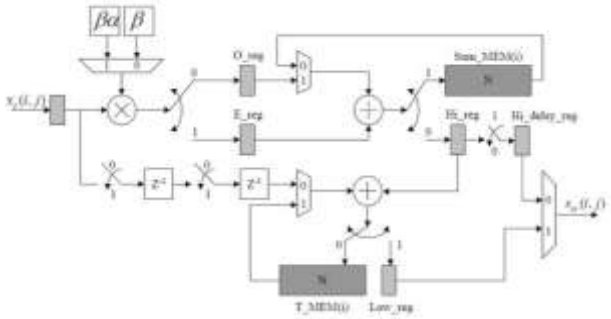

Figure 4.3: 1-D DWT architecture for Row processor

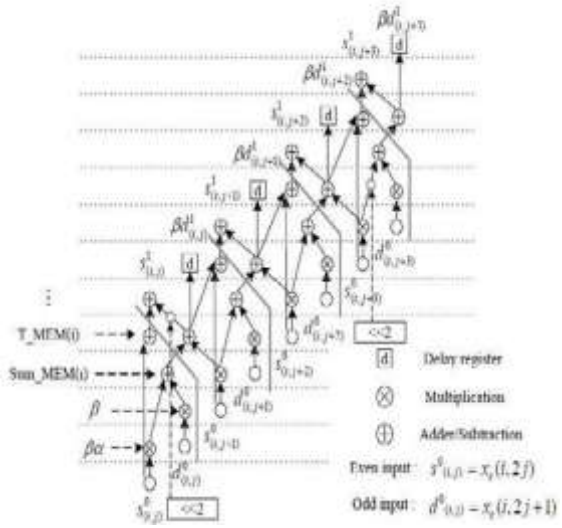


Fig. 4.4 The data path of the i-th column-wise transforms

## VI. SIMULATION AND RESULTS

This section deals with the simulation of Column Processor and Row Processor in XILINX ISE Simulator as well as in MATLAB showing the 2nd level decomposition of image on application of 2D- DWT. The VHDL simulation of all the components used in Row Processor has been described here. The simulated architecture of column processor has also been described here.

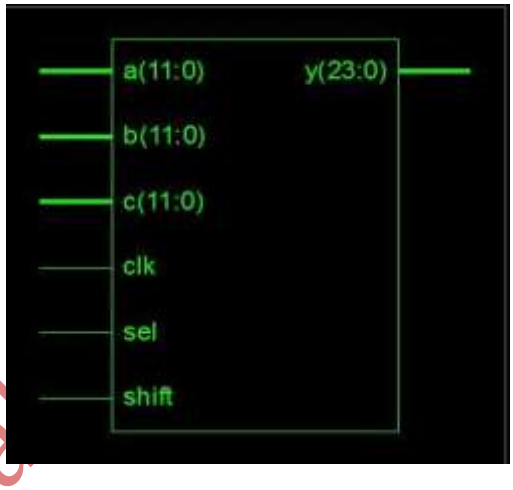


**Figure 5.1: Schematic Symbol of Column Processor in Xilinx**

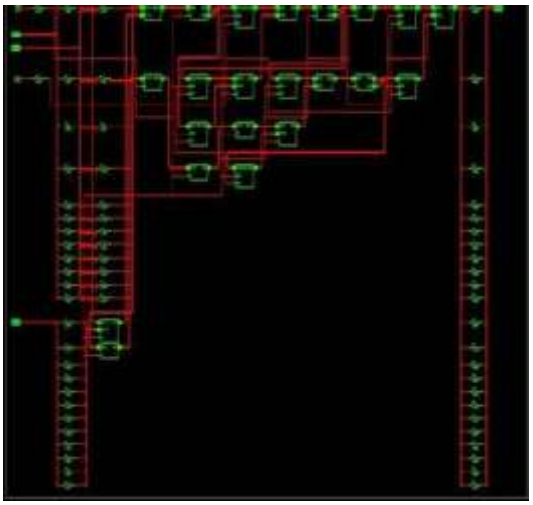

**Figure 5.2: Technology Schematic of Column Processor inXilinx**

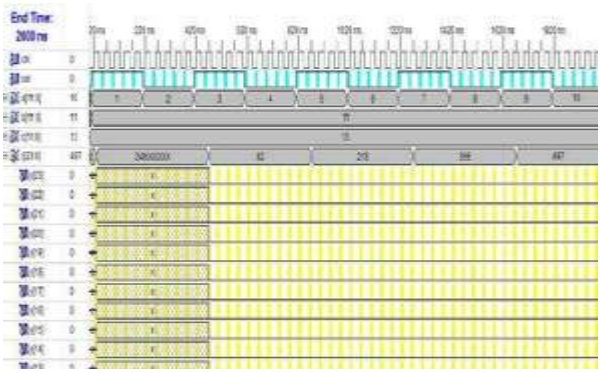

Figure 5.3: Test Bench Waveform of 12 Bit Column Processor.

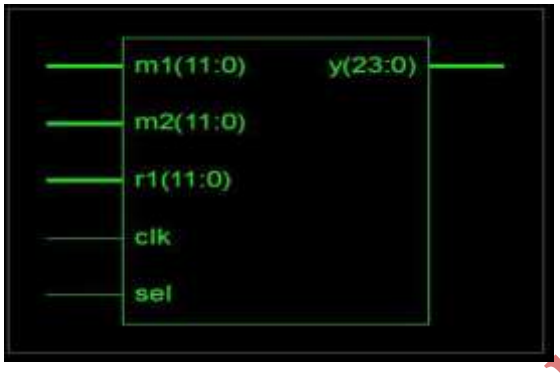


Figure 5.4: Schematic Symbol of 12 Bit Row

Processor in Xilinx

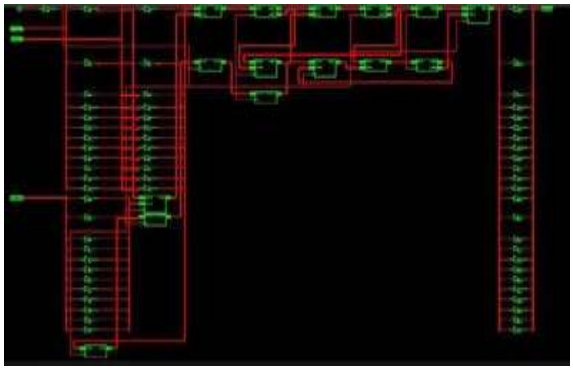

Figure 5.5: Technology Schematic of 12 Bit Row Processor in Xilinx

Figure5.6: Test Bench Waveform of 12 Bit Row Processor in Xilinx

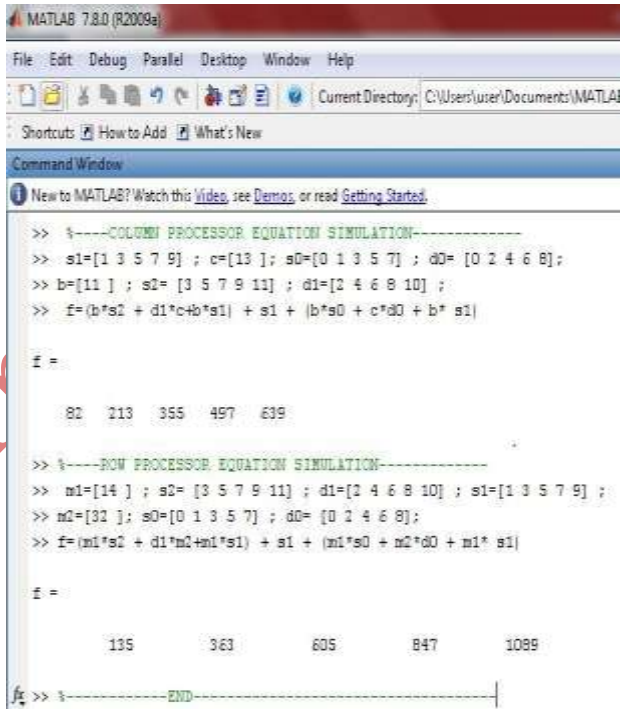


**Figure5.7: Result of CP and RP equation (3.12) simulation in MATLAB**

## VII. CONCLUSION

The Discrete Wavelet Transform gives a multiresolution representation of signs. The change can be executed utilizing channel banks. This paper presents the simulation work for section processor, transposing bufferand line processor of 2D DWT design for JPEG 2000and the investigation of elite and low-memory pipeline engineering for 2-D lifting-based DWT of the 5/3and 9/7 channels. By consolidating the indicator and updater into one single stride, we can

infer effective pipeline design [2]. Henceforth, given the same number of number-crunching units, the given design has a shorter pipeline information way .In this proposal, models for the Lifting based Discrete Wavelet Transform have been executed. For each of them, parameters, for example, memory prerequisite and rate were talked about. Taking into account the application and the limitations forced, the proper design can be picked. The reproduction results check the usefulness of levels of decay can be accomplished the outline. The best possible planning of the wavelet coefficients to the Transposing Buffer guarantees that, when the coefficients are at last read over from the Transposing Buffer, they are accessible in the required request for further preparing by Row Processor. The proposed design [2] is basic since further utilizing indistinguishable preparing components. The engineering empowers quick calculation of DWT with parallel handling. It has low memory prerequisites and expends low power. At long last, the 5/3 and 9/7 channels with the distinctive lifting steps can be acknowledged by falling the three key segments. A superior engineering is acquired by supplanting the multiplier of design with Baugh Wooley multiplier to make it computationally quicker and lesser memory stockpiling necessity.

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