ijournals International Journal of Software & Hardware Research in Engineering
ISSN No: 2347-4890 Volume 2 Issue 1/ January 2014

AN ENHANCED LOW COST HIGH PERFORMANCE IMAGE SCALING PROCESSOR USNIG VLSI

Asha Achenkunju
PG Scholar
Department of Electronics and Communication Engineering,
Sree Sakthi Engineering College,
Coimbatore.

G.Tamilarasan
Assistant Professor
Department of Electronics and Communication Engineering,
Sree Sakthi Engineering College,
Coimbatore.

Dhanesh R
PG Scholar
Department of Electronics and Communication Engineering,
Regional centre,
Anna University, Coimbatore.

ABSTRACT

In this paper, a low complexity, less memory requirement, and high performance algorithm is proposed for Very Large Scale Integration implementation of an image scaling processor. This image scaling algorithm consists of a clamp filter, sharpening spatial filter and a bilinear interpolation. For reducing the aliasing and blurring artifacts resulted by the bilinear interpolation, sharpening spatial and clamp filters are added as pre-filters. T-shaped and inverse T-shaped model convolution kernels are proposed to reduce the memory buffers and also the complexity of the image scalar design. To reduce the computation modules, sharpening spatial and clamp filters are realized by T shaped and inversed T shaped model convolution kernels. Combined filter is replaced by the combination of two T shaped and inversed T shaped model Filters. A reconfigurable calculation unit is presented to minimize the hardware cost of the combined filter. The VLSI architecture in this work is targeted to produce 320 MHz with 6.08-K gate counts. Comparing with Previous techniques, this work improved with respect to cost, performance and less complexity.

General Terms
Bilinear, Clamp filter, Spatial filter, Reconfigurable calculation unit

Keywords
Image zooming, VLSI

1. INTRODUCTION

Image scaling is a non-trivial process that involves a trade-off between efficiency, smoothness and sharpness. As the graphic and video applications of mobile handset devices grow up, the significance of image scaling are more and more outstanding. In computer graphics, image scaling is the process of resizing a digital image. Image scaling has been widely applied in the fields of digital imaging devices and mainly on Electronic based imaging devices. Image scaling is the technique of scaling down the high – quality frames or pictures to fit small size LCD panel of electronic displays such as digital PDA's, mobile phone, or tablet PC. The image scaling algorithms can be classified into two types as polynomial-based and non-polynomial-based methods. The nearest neighbor algorithm is the simplest polynomial-based method. It has the advantage of low complexity, but the resultant images are full of blocking and aliasing artifacts. The bilinear interpolation algorithm is the most widely used scaling method by which the target pixel can be obtained by using the linear interpolation in both of the horizontal and vertical directions. Bi-cubic interpolation algorithm is another popular polynomial-based method, which uses an enhanced cubic model to acquire the resultant pixel by a 2-D regular grid.

Also many high-quality non-polynomial-based methods have been proposed. These novel methods will improve image quality by some efficient techniques, such as curvature interpolation, bilateral filter, and autoregressive model. These techniques efficiently improve the image quality as well as reduce the artifacts of the blocking, aliasing, and blurring effects. But, these high-quality image scaling algorithms are of high complexity and high memory requirement, which is not easy to be realized in VLSI chip. So, for real-time applications, low-complexity, low memory requirement image processing algorithms are necessary for VLSI implementation. For real-time image scaling applications, some previous studies have presented low complexity methods for VLSI implementation. These are the area-pixel model Winscale, and an efficient VLSI design, an area-pixel-based scalar design advanced by an edge-oriented technique, Real-time FPGA architecture of extended linear convolution for digital image scaling, the efficient VLSI design of bi-cubic convolution interpolation for digital image processing, A low-cost high-quality adaptive scalar for real-time multimedia applications. In the previous work, an adaptive real-time, low-cost, and high-performance image scalar using four line buffers was designed. It also improves the image

quality by adding sharpening spatial and clamp filters as pre-filters, by an adaptive technique based on the bilinear interpolation algorithm. Although the memory requirement and hardware cost had been efficiently reduced, it still requires four line buffers. Hence, a low cost, low-area, low-memory-requirement and efficient image scalar design is proposed in this work.

2. RELATED WORKS

2.1) A low-cost high-quality adaptive scalar for real-time multimedia applications

In this paper, a novel adaptive scaling algorithm is used for developing a low-cost, less-power, and high-performance VLSI scaling circuit for image zooming applications. Bilinear interpolation is selected as an interpolation method due to its less complexity and high quality. A clamp filter and a sharpening spatial filter are added as pre-filters to minimize the shortcomings of blurring and aliasing effects caused by the bilinear interpolation. With added adaptive skill, the quality of the resulting scaled images is notably improved.

2.2) Curvature Interpolation Method for Image Zooming

The curvature interpolation method (CIM) uses a novel interpolation algorithm, which is effective in image zooming and easy to implement. The new method is divided into three steps: the evaluation of the curvature from a given LR image, the interpolation of the curvature, and the construction of the zoomed image by solving the curvature equation algebraically. In order to reduce interpolation artifacts, the CIM develops the resulting image, incorporating the interpolated curvature as a driving force, instead of directly interpolating the image itself.

2.3) VLSI implementation of an edge oriented image scaling processor

Image scaling is a very popular technique and has been widely used in many digital imaging applications. In this paper, it presents an edge-oriented area-pixel scaling processor. To achieve low cost, the area-pixel scaling technique is implemented with low-complexity VLSI architecture in the design. A simple edge catching technique is included to enhance the image edge features effectively so as to get better image quality. This work will result a processing rate of 200 megapixels/second for a clock period of 5 ns. The architecture is reliable with both monochromatic and colour images.

2. PROPOSED SOLUTION

In exiting work the memory used is four line buffers. Hence, a low-cost, less-memory-requirement and high performance image scalar design is proposed by using single line buffer as well as to improve the image quality.

3.1) PROPOSED IMAGE SCALING ALGORITHM

Fig.1 represents the block description of the proposed image scaling algorithm. The clamp filter and sharpening filters are added in front of bilinear interpolation as pre-filters in order to reduce the noises resulted by the bilinear interpolation such as blurring and aliasing artifacts. The sharpening spatial filter is used to enhance the edges and remove associated noise and clamp filter is to smooth unwanted discontinuous edges of the boundary regions. The working can be given as the input pixels of the original images are filtered by the sharpening filter and the filtered pixels are filtered again by the combined filter. Finally, the pixels filtered by both of the filters are passed to the bilinear interpolation for up-/ down scaling. To reduce computing resource and memory buffer, the spatial and clamp filters are simplified and combined into a combined filter.

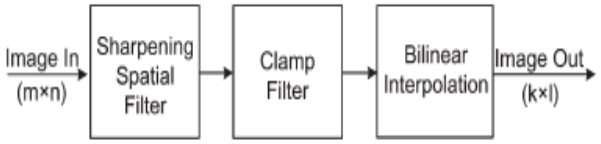

Fig. 1. Block diagram of the proposed scaling algorithm for image zooming.

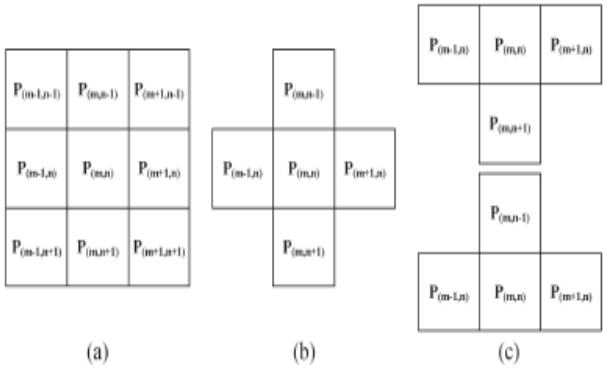

Fig. 2. Weights of the convolution kernels. (a) 3 × 3 convolution kernel. (b) Cross-model convolution kernel. (c) T-model and inversed T-model convolution kernels.

3.2) MODULE DESCRIPTION

The operations of filtering and Image scaling are depends on the processing pixel and size of convolution kernel. These operations can be classified into the following modules.

A) Less complexity Sharpening spatial and Clamp filters.

The sharpening spatial filter is a type of high pass filter, which is used to minimize the blurring artifacts and defined by a kernel. It increases the intensity of a center pixel relative to its neighboring pixels. The clamp filter is a type of low-pass filter. It is a 2-D Gaussian spatial domain filter and composed of a convolution kernel array. It contains a single positive value at the middle and is completely rounded by ones. The clamp filter is used to reduce aliasing artifacts and smooth the unwanted

discontinuous edges of the boundary regions. These sharpening spatial and clamp filters can be represented by convolution kernels. A higher size of convolution kernel will produce higher quality of images. But, a larger size of convolution filter will also demand more memory and hardware cost. For example, a 6 × 6 convolution filter needs at least a five line buffers of memory and 36 arithmetic units, which is much higher than the two-line-buffer memory and nine arithmetic units of a 3 × 3 convolution filter.

In the previous work, each of the sharpening spatial and clamp filters was realized by a 2-D 3 × 3 convolution kernel. It demands at least a four-line-buffer memory for two 3 × 3 convolution filters.

To reduce the complexity of the 3 × 3 convolution kernel, a cross-model is used to replace the 3 × 3 convolution kernel. It successfully cut four of nine parameters in the 3 × 3 convolution kernel. Also to reduce VLSI circuit design complexity of existing cross model convolution kernel, sharpening spatial and clamp filters are realized using T-shaped and inverse T-shaped model convolution kernels. T-model convolution kernel consists of lower four parameters of the cross-model, similarly the inversed T-shaped model convolution kernel is composed of the upper four parameters. In the proposed image scaling algorithm, T-shaped and inversed T-shaped model filters are used for improving the quality of the images simultaneously. This efficiently minimizes the complexity of the convolution filter and greatly reduces the memory requirement from two to one line buffer for each convolution filter. Both the models gives the less area, less complexity and less memory-requirement convolution kernels for the sharpening spatial and clamp filters to integrate VLSI chip of the proposed low-cost image scaling processor.

B) Combined filter

Combined filter is a combination of sharpening spatial and clamp filters. In the proposed image scaling algorithm, first the input image is filtered by a sharpening spatial filter and then filtered by a clamp spatial filter again. The filtered result can be given as

$$P'_{(m,n)} = \left[P^{*}_{(m,n)} \begin{bmatrix} -1 & S & -1 \\ & -1 & \end{bmatrix} /(S-3)\right]^{*} \begin{bmatrix} 1 & C & 1 \\ & 1 & \end{bmatrix} /(C+3)$$

$$= P^{*}_{(m,n)} \begin{bmatrix} -1 & S-C & SC-2 & S-C & -1 \\ & -2 & S-C & -2 & \\ & & -1 & & \end{bmatrix} / [(S-3)\times(C+3)] \quad (1)$$

$$\approx P^{*}_{(m,n)} \begin{bmatrix} -1 & S-C & SC-2 & S-C & -1 \\ & -2 & S-C & -2 & \end{bmatrix} / [(S-3)\times(C+3)] \quad (2)$$

Where S and C are the sharp and clamp parameters. $P\_(m,n)$ is the filtered result of the target pixel $P(m,n)$ by the combined filter. To reduce the one-line-buffer memory, the only parameter in the third line, −1 of $P(m,n-2)$, is removed, and the weight of parameter −1 is added into the parameter S- C of $P(m,n-1)$ by S-C-1. The combined inversed T-model filter can be developed in the same way. In the new Vlsi architecture of the combined filter, any of the two T-model or inversed T-model filters are connected into one combined T-model or inversed T-model filter. By using this filter combination technique, the memory can be efficiently decreased from two to one line buffer, which greatly minimizes memory access requirements for software systems or hardware memory costs for VLSI implementation.

C) Bilinear interpolation

In the proposed image scaling algorithm, the bilinear interpolation method is used because of its efficient characteristics with low complexity and high quality. The bilinear interpolation is a technique that performs a linear interpolation first in x direction and, then again, in y direction. It is the process of finding unknown pixel value in terms of known pixel value. The output pixel P (k,l) can be calculated by the operations of the linear interpolation in both x- and y-directions with the four nearest neighbor pixels. The resultant pixel P (k,l) can be calculated by

$$P_{(k,l)} = (1-dx)\times(1-dy)\times P_{(m,n)} + dx\times(1-dy)\times P_{(m+1,n)} + (1-dx)\times dy\times P_{(m,n+1)} + dx\times dy\times P_{(m+1,n+1)} \quad (3)$$

where $P(m,n)$, $P(m+1,n)$, $P(m,n+1)$, and $P(m+1,n+1)$ are the four nearest neighbor pixels of the original image and the dx and dy are scale parameters in the horizontal and vertical directions.

3.3) VLSI ARCHITECTURE

The proposed image scaling algorithm consists of two combined filters and simplified bilinear interpolator. For VLSI implementation of the proposed design, the bilinear interpolator can directly obtain two input pixels $P\_(m,n)$ and $P\_(m,n+1)$ from two combined filters without any additional line-buffer memory.

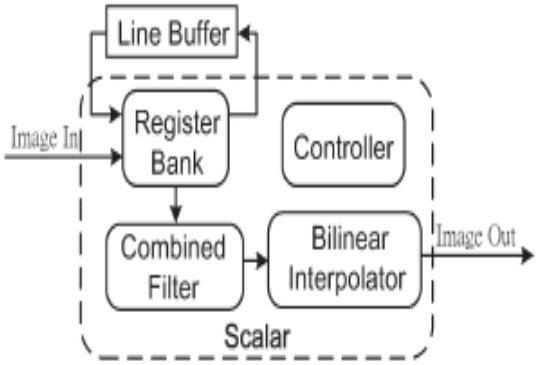

Fig.3 VLSI architecture for proposed real-time image scaling processor.

Fig. 3 shows the block diagram description of the VLSI architecture for the proposed design. The block diagram consists of four main blocks: a register bank with line buffer, a combined filter, a simplified bilinear interpolator, and a circuit controller.

A) Register Bank

The register bank is used for the ordering of the input pixels. It consists of a line buffer. This is used for inputting input pixels to the combined filter and for temporary storage of pixel values.

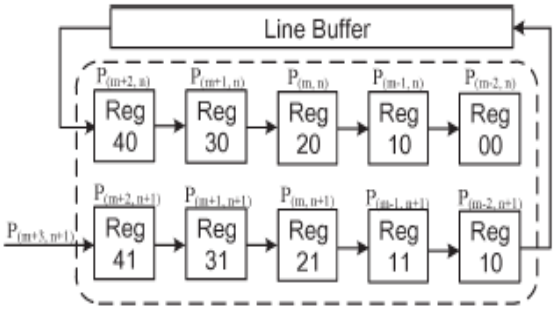

Fig.4 Architecture of Register bank and Line buffer

B) Combined Filter

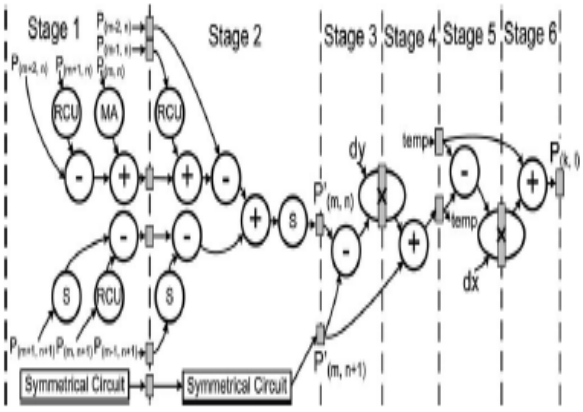

Fig. 5 Computational scheduling of the proposed combined filter and simplified bilinear interpolator.

Fig. 5 shows the six-stage pipelined architecture of the combined filter and simplified bilinear interpolator, which reduces the delay path to increase the performance by pipeline technology. The paths 1 and 2 in Fig. 5 show the computational scheduling of a T-shaped combined and an inverse T-shaped model filter. The T-shaped or inversed T-shaped model filter are realized with three reconfigurable calculation units (RCUs), one multiplier– adder (MA), three adders (+), three subtracters (–), and three shifters (S).

The hardware architecture of the T-model combined filter can be directly mapped with the convolution equation. The values of the ten source pixels can be obtained from the register bank mentioned earlier. The MA can be implemented by a multiplier and an adder. The VLSI architecture of the proposed low-cost, less area combined filter can filter the whole image with only a one line buffer memory. It successfully reduces the memory requirement from four to one line buffer of the combined filter in our previous work.

C) Reconfigurable Calculation Unit

RCU is used for performing filter calculations. The RCU is designed for producing the calculation functions of (S- C) and (S-C-1) times of the input pixel value, which must be implemented with Clamp C and Sharpening S parameters. The Clamp and Sharpening parameters can be set by users.

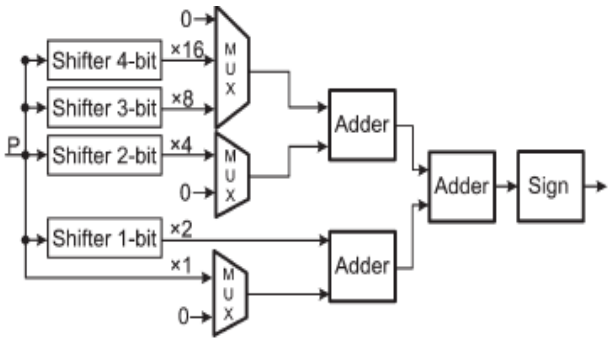

Fig.6 Architecture of RCU

D) Bilinear Interpolator and Controller

Bilinear interpolator is used for image zooming. It is the process of linear interpolation in both x and y directions. The last four stages in Fig.5 show bilinear interpolator architecture. The input values of $P\_(m,n)$ and $P\_(m,n+1)$ are obtained from the combined filter and symmetrical circuit. By the hardware sharing technique, the temperature result of the function "$P\_(m,n) + dy \times (P\_(m,n+1) - P\_(m,n))$" can be replaced by the previous result of "$P\_(m+1,n) + dy \times (P\_(m+1,n+1) - P\_(m+1i,n))$." It also means that one multiplier and two adders can be successfully reduced by adding only one register. Controller is a Finite state machine circuit. This provides control for timing and all blocks in the circuit.

TABLE I
PARAMETERS AND COMPUTING RESOURCE FOR RCU

Parameters	Values	Computing Resource
C	5, 13, 29	Add and Shift
S	7, 11, 19	Add and Shift
S-C	2, -6, -22, 6, -2, -18, 14, 6, -10	Add, Shift, and Sign
S-C-1	1, -7, -23, 5, -3, -19, 13, 5, -11	Add, Shift, and Sign

4) CONCLUSION

In this brief, a minimized cost, less-memory-requirement and high-performance VLSI architecture of the image scaling processor had been proposed. The filter combining, sharing of hardware, and reconfigurable dynamic techniques had been used to reduce hardware cost. Approximating with previous low complexity VLSI image scalar designs, this work achieves at least 34.5% reduction in gate counts and requires only one-line memory buffer.

5) ACKNOWLEDGMENTS

We would earnestly thank our Supervisor for all his valuable comments and active support to our work.

5) REFERENCES

[1] H. Kim, Y. Cha, and S. Kim, "Curvature interpolation method for image zooming," IEEE Trans. Image Process. vol. 20, no. 7, pp. 1895–1903, Jul. 2011.

[2] J. W. Han, J. H. Kim, S. H. Cheon, J.O.Kim, and S. J. Ko, "Anovel image interpolation method using the bilateral filter," IEEE Trans. Consum.Electron., vol. 56, no. 1, pp. 175–181, Feb.2010.

[3] X. Zhang and X.Wu, "Image interpolation by adaptive 2-D autoregressive modeling and soft-decision estimation," IEEE Trans. Image Process., vol. 17, no. 6, pp. 887–896, Jun. 2008.

[4] F. Cardells-Tormo and J. Arnabat-Benedicto, "Flexible hardware-friendly digital architecture for 2-D separable convolution-based scaling," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 522–526, Jul. 2006.

[5] S. Ridella, S. Rovetta, and R. Zunino, "IAVQ-interval-arithmetic vector quantization for image compression," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. vol. 47, no. 12, pp. 1378– 1390, Dec. 2000.

[6] S. Saponara, L. Fanucci, S. Marsi, G. Ramponi, D. Kammler, and E. M. Witte, "Application-specific instruction-set processor for Retinexlink image and video processing," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 7, pp. 596–600, Jul. 2007.

[7] P. Y. Chen, C. C. Huang, Y. H. Shiau, and Y. T. Chen, "A VLSI implementation of barrel distortion correction for wide-angle camera images," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 1, pp. 51–55, Jan. 2009.

[8] M. Fons, F. Fons, and E. Canto, "Fingerprint image processing acceleration through run-time reconfigurable hardware," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 12, pp. 991–995, Dec. 2010.

[9] C. H. Kim, S. M. Seong, J. A. Lee, and L. S. Kim, "Winscale : An image scaling algorithm using an area pixel model," IEEE Trans. Circuits Syst. Video Technol., vol. 13, no. 6, pp. 549–553, Jun. 2003. R.S. KARTHIC, International Journal of Computer Science and Mobile Computing Vol.2 Issue. 4, April-2013, pg. 46-51 © *2013, IJCSMC All Rights Reserved* ***51***

[10] C. C. Lin, Z. C. Wu, W. K. Tsai, M. H. Sheu, and H. K. Chiang, "The VLSI design of winscale for digital image scaling," in Proc. IEEEInt. Conf. Intell. Inf. Hiding Multimedia Signal Process., Nov. 2007, pp. 511–514.

[11] P. Y. Chen, C. Y. Lien, and C. P. Lu, "VLSI implementation of an edgeoriented image scaling processor," IEEE Trans. Very Large Scale integr.(VLSI)Syst., Vol. 17, no. 9, pp. 1275–1284, Sep. 2009.

[12] C. C. Lin, M. H. Sheu, H. K. Chiang, W. K. Tsai, and Z. C. Wu, "Real-time FPGA architecture of extended linear convolution for digital image scaling," in Proc. IEEE Int. Conf. Field-Program. Technol., 2008, pp. 381–384.

[13] C. C. Lin, M. H. Sheu, H. K. Chiang, C. Liaw, and Z. C. Wu, "The efficient VLSI design of BI-CUBIC convolution interpolation for digital image processing," in Proc. IEEE Int Conf. Circuits Syst., May 2008, pp. 480–483.

[14] S. L. Chen, H. Y. Huang, and C. H. Luo, "A low-cost high-quality adaptive scalar for real-time multimedia applications," IEEE Trans. Circuits Syst.Video Technol., vol. 21, no. 11, pp. 1600–1611, Nov. 2011.

[15] K.Jensen and D. Anastassiou, "Subpixel edge localization and the interpolation of still images," IEEE Trans. Image Process., vol. 4, no. 3, pp. 285–295, Mar. 1995.