

Leakage Reduction in Static RAMs: A Survey

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Abstract: *Double-Gate (DG) MOSFET has emerged as one of the most promising devices for logic and memory circuit design. In this paper, we surveyed the Threshold voltage reduction and sub-threshold leakage for DG MOSFET. Then an analysis of the effect of parameter variation to optimize low leakage SRAM cell using DG devices is done. The DG device/circuit co-design successfully demonstrates the benefit of using metal gate intrinsic body DG devices which significantly reduces static power dissipation.*

Keywords: *Double-Gate, sub-threshold, leakage, SRAM.*

1. INTRODUCTION

For over three decades there has been a quadrupling of transistor density and a doubling of electrical performance every 2-3 years. With the anticipation of unconstitutionality of Moore's law within a decade, researchers have embarked in exploring alternative technologies by harnessing the properties of channel materials, dielectric materials and gate work-function engineering that would provide us with high performance with nanoscale devices. Due to excellent control over short channel effects (SCEs), and better "ON" current, DG MOSFETs become one of the promising candidates. However, with continuous downscaling of device dimensions as well as aggressive scaling of oxide thickness, lead to exponential increase of leakage components, which leads to a large stand-by power dissipation. Thus leakage power management becomes indispensable in high-end microprocessors for cost effective solution. We will discuss the leakage components in 6-T SRAM cell using DG device. The total leakage in SRAM cell is substantially reduced using DG devices with sleep transistor. We will also discuss the effect of parameter variation in the DG SRAM cell due to independent gate control and advantage of the using independent gate control in DG devices in circuit design.

2. LITERATURE REVIEW

Investigation of leakage reduction techniques for a conventional 6T SRAM cell in advanced technologies. The most promising leakage reduction techniques that have been proposed are presented and compared for the 130-nm and 65-nm technology nodes. More specifically, the impact of the evolution of the gate tunneling and substrate currents is studied considering the efficiency of those techniques

King Tsu-Jae et al. described important considerations for the sleep transistor (often called MTCMOS) design and implementation including header and footer switch selection, sleep transistor, gate length and width etc. for area, leakage and efficiency and also investigated various power-on current rush control methods for the sleep transistor implementation in which he realized that the two storage charge method is most effective.

Lourts Deepak A. proposed that a Static Random Access Memory works as to plug two applications first cache memory which make communication between central processing unit and dynamic random access memory. Second is the driving force helps to provide the low power applications. SRAM does not require refresh current and it is portable as compared to DRAM.

Mizumura proposed that characteristics V_{th} and I_{on} of driver and load MOSFETs in which SRAM cells is investigated with a new developed SRAM cell array test structure which reported for the first time. The distribution of driver in SRAM cells and load MOSFET characteristics of V_{th} and I_{on} of SRAM cells gives report by using new developed SRAM cell array test structure. SRAM cells of subthreshold humps monitored with algorithm gives occurrence automatically.

Tony Kim et al. said that nowadays CMOS based technologies scale down beyond 90nm or more deep towards submicron level. In this research work,

MOSFET are facing the short channel effect problems that are common in integrated circuits as we move towards the submicron region. Parasitic resistance, capacitance are increases as we reduce the channel length.

The first order continuous turf MOSFET scrambling scheme created model proposed by Shayan Md. which assumed all critical parameters precisely at that level maintained the dignity of its position and significant role in the integrated circuits. The factor that helps to read the scaling effect is dimensionless factor denoted by the S.

$$s=\sqrt{2}$$

The forecast through the International Technology Roadmap for Semiconductors provides the details about the features size in nm vary from 2001 to 2016 is 130 to 22 nm respectively. At 45 nm technology the working is conducted right now and the supply voltage for that feature size is 0.6 to 1.0 V.

Sushil Bhushan et al. presented a 4-T SRAM cell for less power and great compactness applications. The fresh cell size is 35.45% slighter than a standard 6-T cell employing identical design rules. In addition it utilizes one pair bit-line and two word-lines.

Sang Phill Park et al. showed MuGFET (Double-Gate (DG) transistors) appeared out as capable devices for Nano measure circuits as they have good scalability than bulk CMOS devices. Double Gate devices together with liberated gates (separate contacts to front and back gates) have lately been advanced.

Poonam et al. studied the Four-Transistor SRAM Cell in which various parameters like Power dissipation and propagation delay are analyzed in 45nm, 65nm and 90nm technology w.r.t supply voltage V_{dd} and Temperature. The tool used for simulation is TANNER EDA.

Razavipour et al. portrays two SRAM cells in which leakage currents shrinks the static power dissipation. The first cell had a NMOS pass transistors circuit, and the second circuit had PMOS as pass transistors. The total gate leakage of these circuits diminishes as compared to the conventional one.

Then Navakanta Bhat presented a novel SRAM cell which is similar to behavior of Four-Transistor SRAM cell i.e. PMOS has two high load resistors and to regulate the short circuit current with NMOS switch. After simulating the circuit, the energy consumption

becomes lesser as compared to traditional Static RAM cell.

3. CONCLUSION

This paper embarks on a comprehensive quantitative survey towards the simulation of different leakages predominant. We have comprehensively analyzed the DG devices to model the leakages in 6T SRAM cell. Our analysis shows that use of DG devices with sleep transistor can significantly reduce leakage components making it very efficient for constructing SRAM cell. Though threshold voltage is higher in DG devices can efficiently decrease the subthreshold current. As there is no bulk charge for DG, gate-to-channel leakage is also reduced. Hence, we can conclude that DG devices with sleep transistor can emerge as one of the promising candidate for reducing all leakage components making it efficient for low power circuit design.

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