

# Design and Implementation of DG-MOSFET based Low Leakage S-RAM on 90nm CMOS

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**ABSTRACT:** The paper presents a 6T SRAM based on DG-MOSFET and Sleep Transistor for leakage current reduction. A bulk 6T SRAM is implemented and simulated for the proper functioning of the SRAM cell for 1 bit storage on the 90nm technology. We have used a DG-MOSFET for reducing the threshold voltage and so the power consumption. On the circuit level, the static power dissipation has been considered. Reduction of leakage current is done by using Sleep Transistor technique. The DG-MOSFET based 6T SRAM with Sleep Transistor technique is implemented and simulated. The designing and simulation tool we used is Cadence virtuoso. The transient, dc and parametric analysis provide the results. The transient response helps to show the proper function of SRAM and dc response provides the results related to the voltage values which are helpful to know about the power consumption of the circuit. The parametric analysis gives different values of leakage current on different width of the MOSFET which shows that the bulk 6T SRAM consumes more power than DG-MOSFET based 6T SRAM with Sleep Transistor. It has been shown that proposed circuit performs substantially better compared to the conventional SRAM in regards of leakage reduction.

**Keywords:** Static RAM, Leakage Current, Bulk 6T SRAM, DG-MOSFET, Sleep Transistor.

## I. INTRODUCTION

Recent memory technologies including SRAM, DRAM and flash memory are facing technology limits to their continued upgrading. Accumulation of new materials to improve gate SiO<sub>2</sub>oxide concert and consistency can only add to circuit costs. This fact has led to intense efforts to ripen new memory technologies. This type of memory which addressed is primary and secondary memory which is volatile but BIOS battery helps to provide them power supply to be in hold mode. Most of these new technologies are less affected by short channel effect on memories and can be used for long term storage or to provide a memory that does not lose information automatically. DG-MOSFET based SRAM cells will begin a new substitute to CMOS based SRAM and DRAM cells in a next few years.

The rate of development of compact memories more and more with fewer amounts of its drawbacks helps to replace CMOS technologies to DG-MOSFET based emerging technologies. Moving to a DG-MOSFET based disk and cache devices will reduce power usage and dissipation directly as well as with new power saving modes, and it provides the better performance in lesser channel length. The use of a double gate technology as an embedded memory with CMOS logic has countless job the electronics industry.

## II. IMPLEMENTATION AND DESIGN 6T SRAM Cell

As SRAM cell is the most traditional circuit in system on chip (SoC) technology which scales down size of cell and also voltage. 6T SRAM

cell have total of six transistors in which four are NMOS and two are PMOS. Out of six, four transistors i.e. NMOS and PMOS transistors combines to form a pair of inverters in bi-stable latched format and the other two NMOS transistors (N3 & N4) are used to pass bit line data in bi-stable latched that shown in Figure 1.

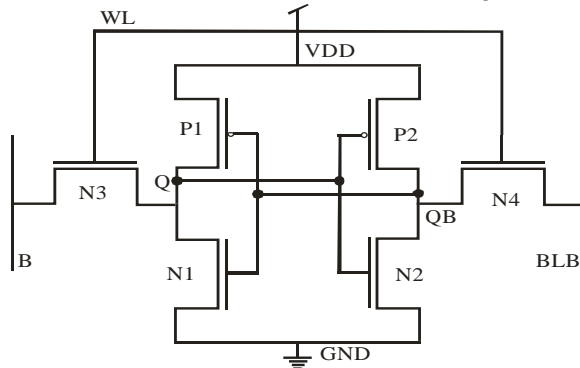


Figure 1 Conventional 6T SRAM Cell

In 6T SRAM Cell there are two bit lines BL and BLB which are complement of each other but of same period and Q and QB are also complemented outputs and a single word line WL. There are three modes of operation in SRAM cell i.e. Hold mode, active mode, stand-by mode. In stand-by mode WL goes high to low (WL=0) and the bit line either 0 or 1, it just holds the data inside the cross coupled inverters. In write mode, word line goes low to high (WL=1) and new data is put into BL bit line, that data writes on Q and QB outputs using pass transistors. When word line goes high to low (WL=0) and the data on bit line (BL) is pre-charged or left floating, the value stored during write operation at output Q goes through pass transistor to one of bit line that is discharging and another one line is pre-charging and this charging and discharging of data is sense by sense amplifier during read operation and amplifies the data which is used further at outputs Q and QB.

### PROPOSED DG-MOSFET BASED SRAM CELL

The memory design is very simple just to hold single bit data. The memory that we are using in our application purpose is the 1-bit of memory due to that data retention and power dissipation

in are major issues, so future requires technology which has scaling capability itself to reduce size because of that DG--MOSFET becomes point of line for this issue. For better reduction in short channel effects, power supply scaling capability, low power dissipation, DG-MOSFET is superior choice than conventional CMOS.

The MuGFET based CMOS technology on SRAM cell and E-memory that helps to cell stability issues, reduced leakage current, and better device mismatch. The low power design is suitable through DG-MOSFET due to no body biasing for leakage reduction and it works on less power supply voltage compare to CMOS logic.

DG-MOSFET width needed efforts to design SRAM cell by adjusting  $V_{th}$  of SRAM cell. So we design 6T SRAM cell using model and studied in different voltages.

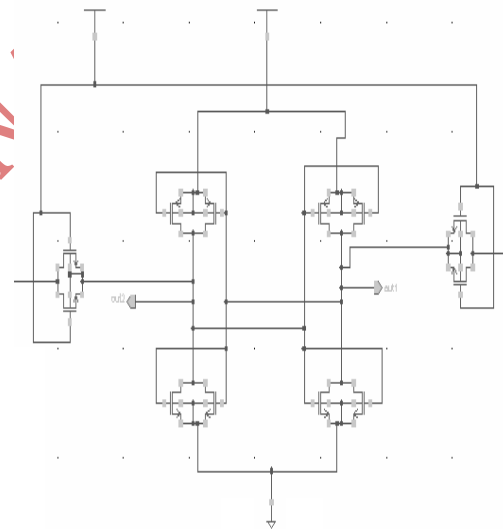


Figure 2 DG-MOSFET based 6T SRAM Cell

### Leakage current

One of the most important characteristics of ideal CMOS technology is the fact that it doesn't exhibit any magnitude of static power dissipation in steady state. In practical situations though, degraded levels of voltage are fed to gate comprising of CMOS transistors and a subsequent flow of current can be seen from power supply to ground, which is often termed as static biasing current. In Fig. 4, depicts the situation in which an inverter is driven by a pass

transistor. On analyzing the circuit, we reach to the result that voltage at node A is degraded ( $V_{dd}-V_{th}$ ). The inverter input being high ( $V_{dd}-V_{th}$ ), the output would be low. Since, the PMOS transistor is weakly ON which results in static biasing current from power supply to ground nodes. Thus static biasing current come into the picture due to the aforesaid conditions. Static currents which flow from  $V_{dd}$  to ground, without degrading the inputs is known as leakage power. With the advent of technology resulting in scaling, supply voltage must be reduced to address dynamic power and issues pertaining to reliability. This in turn needs scaling of the device threshold voltage ( $V_{th}$ ) so that a reasonable gate over drive can be maintained. Reduction in  $V_{th}$ , results in the subthreshold current to increase exponentially.

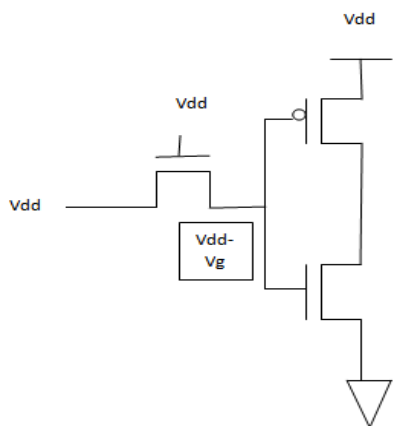


Figure4 Degraded voltage level at the input node of a CMOS inverter results in static biasing power consumption

During the condition  $V_{gs} < V_{th}$ , the NMOS is off-state. Still, an unwanted value of leakage current might flow from the drain terminal to the source terminal. The current observed in the MOSFET at  $V_{gs} < V_{th}$  is called the subthreshold current. This subsequently results in MOSFET off-state current,  $I_{off}$ .  $I_{off}$  is the  $I_d$  measured at  $V_{gs}=0$  and  $V_{ds}=V_{dd}$ . It becomes mandatory for  $I_{off}$  to have a very small value so that the circuit consumes negligible static power (typically in stand by mode)

As an illustration, let us consider  $I_{off}$  be 100nA per transistor, a simple cell-phone chip that

contains 100,000,000 transistors would consume almost a standby current (10A) that would result in the battery draining out briskly even without the cell phone getting any call. A desk-top computer may still be used but at the cost consuming power from the a.c. mains supply or UPS and moreover causing excessive heating problems. When  $V_{gs}$  is below  $V_{th}$ ,  $I_{ds}$  behaves as an exponential function of  $V_{gs}$ .

Fig. 5 depicts the subthreshold current. When  $V_{gs}$  is below  $V_{th}$ , the concentration of inversion electron ( $n_s$ ) is quite small but still it can result in a small leakage current to flow between the source and the drain terminals. In Fig.5, a large value of  $V_{gs}$  would pull  $E_c$  at the surface closer to  $E_f$ , causing  $n_s$  and  $I_{ds}$  to increase. From the equivalent circuit in Fig. 5 (b), it can be observed that:

$$\frac{d\phi_s}{dV_{gs}} = \frac{C_{oxe}}{C_{oxe} + C_{dep}} \equiv \frac{1}{\eta} \quad (6)$$

$$\eta = 1 + \frac{C_{dep}}{C_{oxe}} \quad (7)$$

Integrating Eq. (6) yields

$$\phi_s = constant + \frac{V_g}{\eta} \quad (8)$$

$I_{ds}$  is proportional to  $n_s$ , therefore

$$I_{ds} \propto n_s \propto e^{\frac{q\phi_s}{kT}} \quad (9)$$

$$\propto e^{q(constant + \frac{V_g}{\eta})} \propto e^{\frac{qV_g}{\eta kT}} \quad (10)$$

The practical definition of  $V_{th}$  in experimental studies is the  $V_{gs}$  at which  $I_{ds}=100nA \times W/L$ . (Some companies may use 200nA instead of 100nA.) Eq. (9) may be rewritten

$$I_{ds} (nA) = 100 \cdot \frac{W}{L} \cdot e^{\frac{q(V_{gs} - V_{th})}{\eta kT}} \quad (11)$$

Clearly, Eq. (10) agrees with the definition of  $V_{th}$  and Eq. (9). Considering the fact that the function  $\exp(qV_{gs}/kT)$  changes by 10 for every 60 mV change in  $V_{gs}$ , hence  $\exp(qV_{gs}/\eta kT)$  changes by 10 for every  $\eta \times 60mV$ . As an illustration, if  $\eta=1.5$ , Eq. (10) states that  $I_{ds}$

drops by 10 times for every 90mV of decrease in  $V_{gs}$  below  $V_t$ .  $h \times 60mV$  is called the subthreshold swing and represented by the symbol,  $S$ .

$$S = \eta \cdot 60 \text{ mV} \cdot \frac{T}{300} \quad (12)$$

$$I_{ds} (\text{nA}) = 10 \frac{W}{L} e^{\frac{q(V_{gs} - V_{th})}{\eta kT}} \quad (13)$$

$$I_{off} (\text{nA}) = 100 \frac{W}{L} 10^{\frac{-V_{th}}{S}} \quad (14)$$

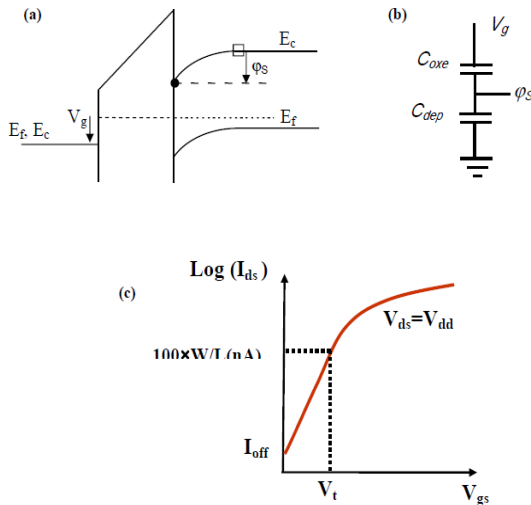


Figure 5: (a) When  $V_g$  is increased,  $E_c$  at the surface is pulled closer to  $E_f$ , causing  $n_s$  and  $I_{ds}$  to rise; (b) equivalent capacitance network; (c) Subthreshold IV with  $V_t$  and  $I_{off}$

There are two ways to minimize  $I_{off}$  illustrated for some given value of  $W$  and  $L$  shown in Fig. 5 (c). One is choosing a large value of  $V_{th}$ , but this is not an optimal solution since it would reduce  $I_{on}$  and hence increase the gate delays. The other more feasible solution is to reduce the subthreshold swing ( $S$ ).  $S$  can be reduced by reducing  $h$ . That can be done by increasing  $C_{oxe}$  (see Eq. 7), i.e. using a thinner  $T_{ox}$ , and by decreasing  $C_{dep}$ , i.e. increasing  $W_{dep}$ . Another way to reduce  $S$  is to reduce  $I_{off}$ , so that the transistors operate at a lower temperature. The last mentioned technique is seldom used for the additional cost that cooling needs.

### III. SIMULATION AND RESULTS

The simulation can be tested on the following EDA tools:

- 1) Cadence Virtuoso
- 2) EDA Tanner
- 3) Microwind.

The standardized models have been designed and tested based on the Cadence Virtuoso tool on the 90nm CMOS technology.

We represent the simulation waveform of the three types of analysis:

1. Transient Analysis of the input and output circuits.
2. DC Analysis of the DC voltage source.
3. Leakage current Analysis

All the above analysis are done for four types of circuit, first is the 6T SRAM, second is the DG-MOSFET based 6T SRAM, third is 6T SRAM with Sleep Transistor and DG-MOSFET based 6T SRAM with Sleep Transistor.

We also compare the bulk 6T SRAM and DG-MOSFET based 6T SRAM with and without Sleep Transistor by the variation of the feature size.

By doing all the above analysis and comparison we can easily find the precise applicability of the circuit in different VLSI systems. The analysis and comparison provides the better performance of DG-MOSFET based 6T SRAM over Bulk SRAM with Sleep Transistor technique so that we prefer DG-MOSFET based 6T SRAM with Sleep Transistor technique for getting low power dissipation.

Figure 7 shows the circuit of the bulk 6T SRAM cell and Figure 8 shows the proposed DG-MOSFET based 6T SRAM cell. Figure 9 shows the transient response of the bulk 6T SRAM cell and Figure 10 shows response of the proposed DG-MOSFET based 6T SRAM cell by cadence virtuoso tool using the process technology at 90nm, with the minimum supply voltage 0.7V.

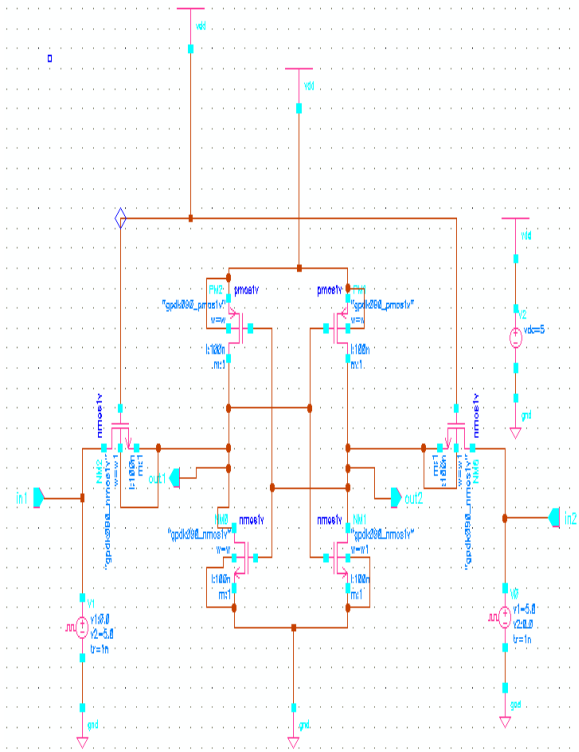


Figure 7 Circuit of the bulk SRAM Cell

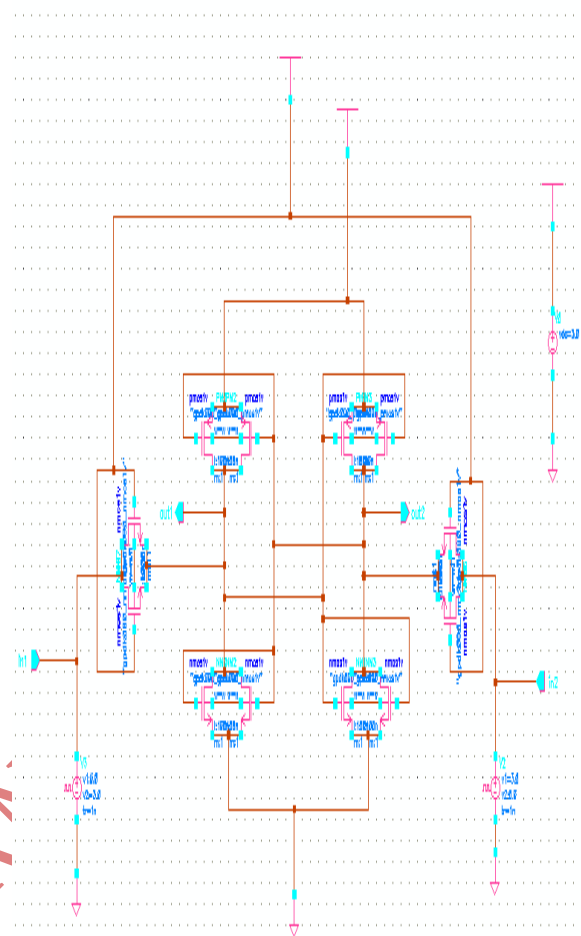


Figure 8 Circuit of the DG-MOSFET Based 6T SRAM Cell

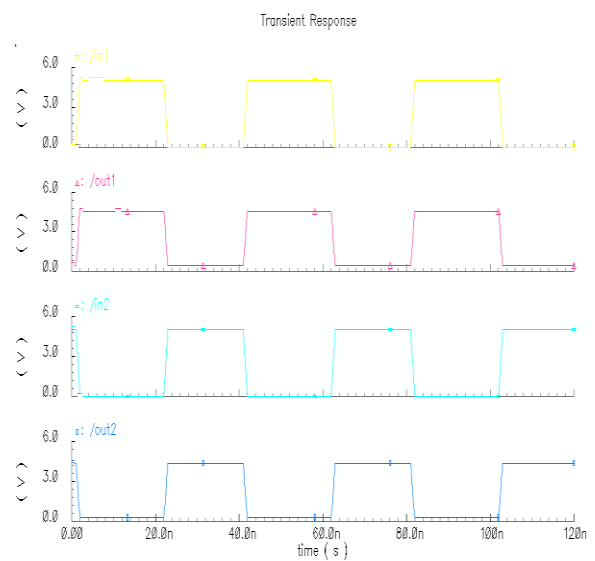


Figure 9 Transient Response of the bulk SRAM Cell

The above simulation result shows that the bulk 6T SRAM works well as it stores 1 bit of data according to the input pulse range. In the diagram four waveforms are shown. First waveform is the input to the SRAM of the range 0 to 5V for 120ns. The second waveform is the output of the first waveform which is same as input and provide accurate information to the output. The third waveform is the second input to the SRAM of the range 5 to 0V for 120ns. The fourth waveform is the output of the first waveform which is same as second input but invert of the first input which is required according to the functionality of the SRAM.

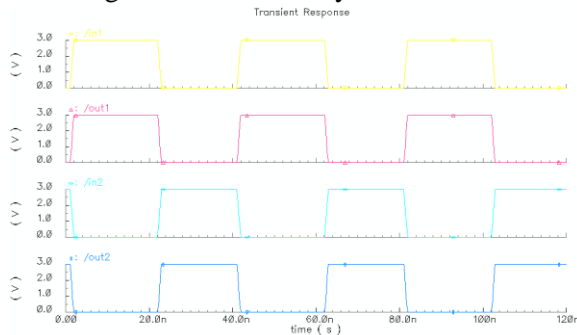


Figure 10 Transient Response of the Proposed DG-MOSFET Based 6T SRAM Cell

The above simulation result shows that the DG-MOSFET based 6T SRAM works well as it stores 1 bit of data according to the input pulse range. In the diagram four waveforms are shown. First waveform is the input to the DG-MOSFET based 6T SRAM of the range 0 to 3V for 120ns. The second waveform is the output of the first waveform which is same as input and provide accurate information to the output. The third waveform is the second input to the DG-MOSFET based 6T SRAM of the range 3 to 0V for 120ns. The fourth waveform is the output of the first waveform which is same as second input but invert of the first input which is required according to the functionality of the SRAM.

From the above two circuits it is clear that the circuits work well and the function of the SRAM are perfect in both of them.

Figure 11 shows the transient response of the bulk 6T SRAM cell and Figure 12 shows response of the proposed DG-MOSFET based 6T SRAM cell.

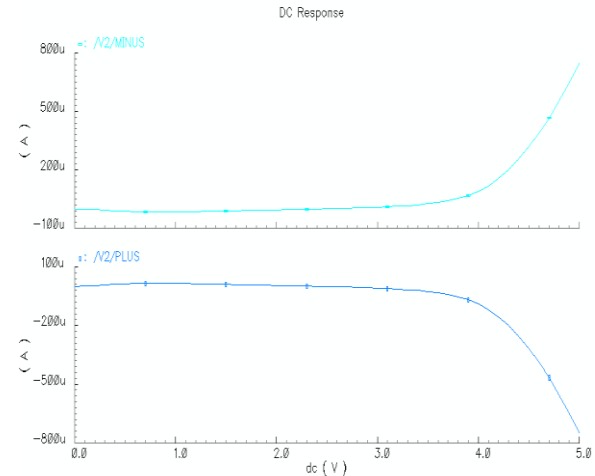


Figure 11 DC Response of the bulk SRAM Cell From the above figure it is seen that the applied dc voltage to the circuit is 5V. The two waveforms are shown in which first one is the values getting from the negative terminal of the dc voltage source and the second one is from the positive terminal of the dc voltage source.

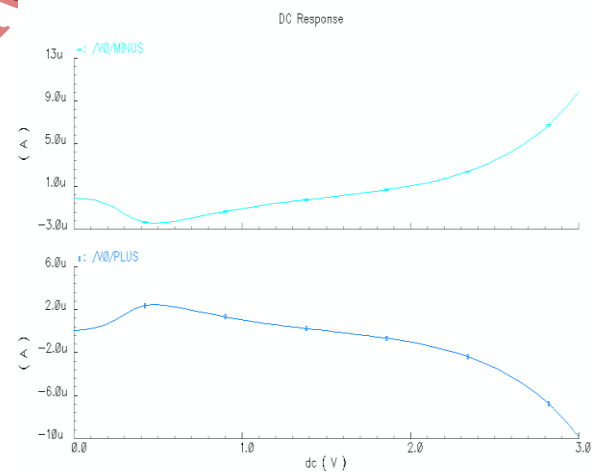


Figure 12 DC Response of the Proposed DG-MOSFET Based 6T SRAM Cell

From the above figure it is seen that the applied dc voltage to the circuit is 3V. The two waveforms are shown in which first one is the values getting from the negative terminal of the dc voltage source and the second one is from the positive terminal of the dc voltage source.

Now the leakage current is being calculated. As we know that the leakage current is the sum of diffusion and subthreshold current so that the waveforms we are getting from the circuits are given the combined value of the both.

Figure 13 shows the circuit of the bulk 6T SRAM cell and Figure 14 shows the proposed DG-MOSFET based 6T SRAM cell with sleep transistor.

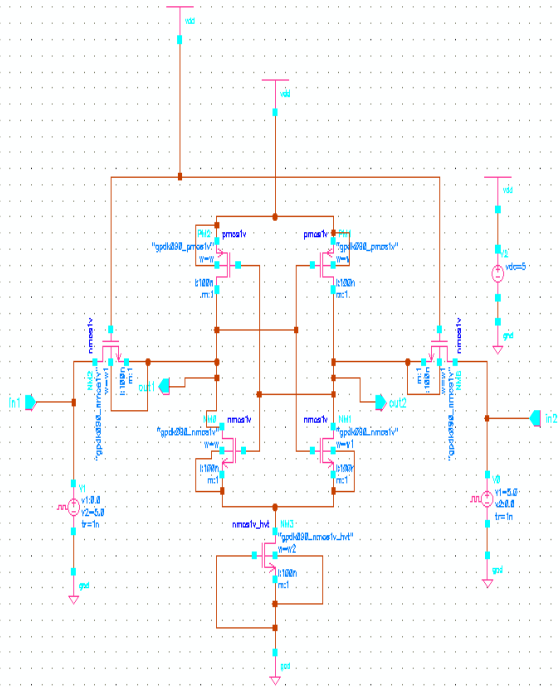


Figure 13 Circuit of the bulk SRAM Cell with sleep transistor

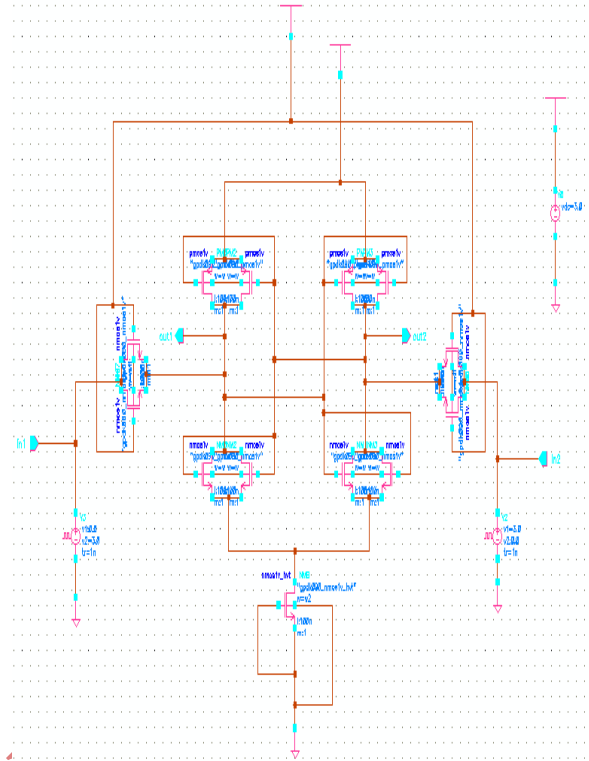


Figure 14 Circuit of the DG-MOSFET Based 6T SRAM Cell with sleep transistor

For getting leakage current of the circuit we are selecting a point of Sleep Transistor. As we know that in the Sleep Transistor the source terminal of the NMOS is connected to the ground so that we can get the value of leakage current from this node of the SRAM circuit.

The comparison table of leakage current for the different values of MOSFET width is given below:

Table 1: Leakage current values with Sleep Transistor at 90nm technology

W/L = x/100	AT THE SOURCE NODE OF	BULK 6T SRAM	DG- MOSFET BASED 6T SRAM
x = 450nm	NMOS	508.20pA	19.101pA
x = 500nm	NMOS	548.46pA	20.557pA
x = 550nm	NMOS	587.76pA	22.057pA
x = 600nm	NMOS	628.40pA	23.519pA

x = 650nm	NMOS	668.78pA	25.016pA
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From the Table 1, we can see that by using different feature sizes, we can get different values of the leakage current. As the width of the MOSFET of the bulk 6T SRAM is increased, the leakage current is reduced. The same is done with the DG-MOSFET based SRAM. When we compare the values of leakage current of the bulk 6T SRAM with DG-MOSFET based 6T SRAM, reduction in the leakage current is found which is depicted by the corresponding waveforms.

#### IV. CONCLUSION

**It can be concluded from previous discussions that it is necessary to reduce the leakage of SRAMS so as to reduce the power consumption. A 6T SRAM has been designed using the 90nm DG MOS and Sleep Transistor for leakage reduction. The transient, dc and parametric analysis provide the results. The transient, dc and parametric analysis have been conducted. The parametric analysis gives different values of leakage current on different width of the MOSFET which shows that the bulk 6T SRAM consumes more power than DG-MOSFET based 6T SRAM with Sleep Transistor. It has been shown that proposed circuit performs substantially better compared to the conventional SRAM in regards of leakage reduction.**

#### References

[1] Teh YK, Mohd-Yasin F, Choong F, Reaz MI, Kordesch AV, "Design and analysis of UHF micropower CMOS DTMOST rectifiers", IEEE Transactions on Circuits and Systems II: Express Briefs; vol.56, no.2, pp.122-126, 2009.

[2] Chandrakasan, Anantha P., and Robert W. Brodersen, "Minimizing power consumption in digital CMOS circuits," In Proceedings of the IEEE, vol.83, no.4, pp.498-523, 1995.

[3] Thomas Oliver, "Impact of CMOS technology scaling on SRAM standby leakage reduction techniques", IEEE International Conference on Integrated Circuit Design and Technology, 2006.

[4] Singh R., Pattanaik M., and Shukla N., "Characterization of a Novel Low-Power SRAM Bit-Cell Structure at Deep Sub-Micron CMOS Technology for Multimedia Applications," Circuits and Systems Scientific Research, vol. 3, no. 1, pp. 23-28, 2012.

[5] E. Grossar, "Technology-aware design of SRAM memory circuits," Technical Note, pp.226, 2007.

[6] Upadhyay Prashant, R. Mehra, and Niveditta Thakur, "Low power design of an SRAM cell for portable devices", International Conference on Computer and Communication Technology (ICCCCT), pp. 255-259, 2010.

[7] Jadav, Sunil, and Munish Vashisath. "Design and Performance Analysis Of Ultra Low Power 6T SRAM Using Adiabatic Technique", arXiv preprint arXiv:1207.3302, 2012.

[8] Alireza Shafaei, Yanzhi Wang, Xue Lin, and Massoud Pedram, "Fin CACTI: Architectural Analysis and Modeling of Caches with Deeply-scaled FinFET Devices," IEEE Computer Society Annual Symposium on VLSI, pp. 290-295, 2014.

[9] L. Chang et al., "Stable SRAM Cell Design for the 32nm Node and Beyond," Symp. VLSI Tech. Dig., pp. 292-293, Jun., 2005.

[10] Rafik S. Guindi, Farid N. Najm, Design Techniques for Gate-Leakage Reduction in CMOS Circuits, Proceedings of the Fourth International Symposium on Quality Electronic Design, p.61, March 24-26, 2003.

[11] Kim Nam Sung, Todd Austin, D. Baauw, Trevor Mudge, Krisztián Flautner, Jie S. Hu, Mary Jane Irwin, Mahmut Kandemir, and Vijaykrishnan Narayanan, "Leakage current: Moore's law meets static power", Computer, vol.36, no.12, pp.68-75, 2003.

[12] Tsai Y-F., David Duarte, Narayanan Vijaykrishnan, and Mary Jane Irwin, "Implications of technology scaling on leakage reduction techniques", In Proceedings of IEEE in Design Automation Conference, pp: 187-190, 2003.

[13] Lee David Blaauw, and Dennis Sylvester, "Gate oxide leakage current analysis and reduction for VLSI circuits", IEEE Transactions on VLSI, vol. 12, no.2, pp.155-166, 2004.

[14] Achiranshu Garg and Tony Tae-Hyoung Kim, "SRAM Array Structures for EnergyEfficiency Enhancement," IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II:, VOL. 60, NO. 6, JUNE 2013, pp. 351-355.

[15] Sushil Bhushan, Shishir Rastogi, Mayank Shastri, Shyam Akashe and Sanjay Sharma, "High Density Four-Transistor SRAM Cell with Low Power

Consumption," International Journal of Computer Technology and Applications, vol.2, no. 5, 2011.

[16] Poonam, Sonika Soni, and Manoj Taleja. "Comparative Analysis of Nano Scaled Low Power 4T SRAM Cell at Various Technology Nodes."

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