

# Efficient Clocking System with Low Power Consumption Using Clocked Pair Shared Flip flop

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**Abstract**— The clock system consisting of clock distribution networks and sequential elements is most power consuming VLSI components. Reductions of flip flop, power consumption have a deep impact on the total power consumption. Since power consumption is a major bottleneck of system performance, the clock load should be reduced to reduce the power consumption. The clock distribution network distributes the clock signal from a common point to all the elements that need it. Since this function is vital to synchronous system, much attention has been given to the characteristics of these clock signal and the electrical networks used in their distribution. In synchronous system clock distribution networks consumes a large amount of total power because of high operation frequency of highest capacitance. An effective way to reduce capacity of clock load is by minimizing number of clocked transistor. In low swing differential capturing flip flop system clock distribution networks consumes a large amount of chip power and there exist a more number of clocked transistor. Hence by a novel approach, clocked paired shared flip flop is used to reduce the number of local clocked transistors.

**Keywords**— *synchronous system; low swing differential capturing flip flop; clocked transistor*

## I. INTRODUCTION

Digital logic is the foundation for digital computers, to understand the innards of computers. There are a number of different systems for representing binary information in physical systems. A voltage signal with zero (0) corresponding to '0' volts and one (1) corresponding to five or three volts. VLSI is the field which involves packing more and more logic devices into smaller and smaller areas. This has opened up a

big opportunity to do things that were not possible before. Resonant clocking is an emerging promising technique to reduce the power of the clock network. The inductor used in resonant clocking enables the conversion of the electric energy stored on the clock capacitance to magnetic energy in the inductor and vice versa.

The concept of the slack in the clock skew has been extended for an LC fully-resonant clock distribution network [11]. This extra slack in comparison to standard clock distribution networks can be used to reduce routing complexity, achieve reduction in wire elongation, total wire length, and power consumption.

## II. RELATED WORK

Seyed E. Esmaeili Rttl. has proposed conditional capturing which is used to minimize power at low data switching activities by eliminating redundant internal transitions. Reduced swing inverters similar to the one presented in is used at the node fed by the low swing [3] sinusoidal clock signal. This is done to reduce short circuit power. The load pMOS transistor in the reduced swing inverters is always in saturation since  $V_{gs}=V_{ds}$ . It lowers the voltage at the source of the second pMOS in each inverter to approximately  $V_{DD}-|V_{tp}|$  thus turning it off when the low-swing sinusoidal clock signal reaches its peak voltage.

S.E. Esmaeili A.J. Al-Khalili G.E.R describes the differences in the results for the TDQ response of the dual edge triggered flip-flop at the positive and negative clock edges obtained from schematic and post-layout simulations. The resonant sinusoidal clock signal becomes a square wave clock when inverted using an inverter. The effect of the long rise time of the positive edge of the sinusoidal clock signal CLK1, which defines the start of the first evaluation interval TE1, compared to the effect of the short rise time of the inverted square signal CLK2, which defines the start of the second evaluation interval TE2, on the

TDQ delay against TDCLK delay (Tsetup) is investigated. In this paper we introduce a new flip-flop for use in a low-swing LC resonant clocking scheme. The proposed low-swing differential conditional capturing flip-flop (LS-DCCFF) operates with a low-swing sinusoidal clock through the utilization of reduced swing inverters at the clock port. The functionality of the proposed flip-flop was verified at extreme corners through simulations with parasitics extracted from layout. The LS-DCCFF enables 6.5% reduction in power compared to the full-swing flip-flop with 19% area overhead. In addition, a frequency dependent delay associated with driving pulsed flip-flops with a low-swing sinusoidal clock has been characterized. The LS-DCCFF has 870 ps longer data to output delay as compared to the full-swing flip-flop at the same setup time for a 100 MHz sinusoidal clock. The functionality of the proposed flip-flop was tested and verified by using the LS-DCCFF in a dual-mode multiply and accumulate (MAC) unit fabricated in TSMC 90-nm CMOS technology. Low-swing resonant clocking achieved around 5.8% reduction in total power with 5.7% area overhead for the MAC.

### III. SURVEYED TECHNIQUE FOR REDUCING CLOCK CAPACITY

Most of the flip-flops presented here are dynamic in nature, and some internal nodes are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable. Reducing this redundant switching activity has a profound effect in reducing the power dissipation, and in the literature many techniques were presented for this purpose. A brief survey of such techniques is conducted in this work, and the main techniques were classified as follows:

#### 3.1 Conditional Capture Flip Flop

Conditional Capture technique is proposed for disabling redundant internal transitions. This technique achieves significant power reduction at little or no delay penalties. Motivation behind Conditional Capture technique[3] is the observation that considerable portion of power is consumed for driving internal nodes even when the value of the output is not changed (corresponding to low input activities). It is possible to disable internal transitions when it is detected that they will have no effect on output. But the drawback is increased set-up time for sampling zero (low level) and also heavier load is presented to the Q output of the flip flop.

#### 3.2 Conditional Precharge Flip Flop

For overcoming the disadvantage in Conditional Capture Flip Flop[3], Conditional pre-charge flip flop is proposed. One of the most important contributions of this work is related to preventing unconditional pre-charge operation of the internal node, tightly connected to excessive power dissipation of the circuit. This is

accomplished by controlling the return of internal node to inactive (high) state, allowing the internal node to stay at low level until input condition is changed. This approach efficiently eliminates the unnecessary transitions of the internal node as well as race condition at the output. There are two main disadvantages: One is introducing another critical path for low input level capture. Another drawback is increasing the output load due to the feedback, which although minimal size transistor can be used, being out of the critical path, can affect total propagation delay.

#### 3.3 Conditional Discharge Flip Flop

Conditional Discharge Flip-flop (CDFF)[4] not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small Q-to-output delay characteristics. With a data-switching activity of 37.5%, this flip-flop can save up to 39% of the energy with the same speed. In this Flip-flop, the extra switching activity is eliminated by controlling the discharge path when the input is stable HIGH. In this scheme, an n-MOS Transistor is inserted in the discharge path with the high-switching activity. When the input undergoes a LOW-to-HIGH transition, the output changes from HIGH to LOW. This transition at the output switches off the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable. But the disadvantage is it used 15 clocked transistors.

#### 3.4 Conditional Data Mapping Flip Flop

A large part of the on-chip power is consumed by the clock drivers. It is desirable to have less clocked load in the system. CDFF and CCFF both have many clocked transistors. For example, CCFF used 14 clocked transistors, and CDFF used 15 clocked transistors. In contrast, conditional data mapping flip-flop (CDMFF, Fig3.1) used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFF. (Note that CDFF used double edge clocking. For simplicity purposes, we did not include the power savings by double edge triggering on the clock distribution network). This shows the effectiveness of reducing clocked transistor numbers to achieve low power. Since CDMFF outperforms CCFF and CDFF in view of power consumption,

However, there is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the precharging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path because its first stage is dynamic. When clock signal CLK transits from 0 to 1, CLKDB will stay 1 for a short while which produces an implicit pulse window for evaluation. During that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be

disconnected by N3 using data mapping scheme (N6 turns off N3); If D is 0, the pull down network is disconnected from GND too. Hence internal node X is not connected with Vdd or GND during most pulse windows, it is essentially floating periodically. With feature size shrinking, dynamic node is more prone to noise interruption because of the undriven dynamic node. If a nearby noise discharges the node X, pMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nanoscale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment. Unlike CDMFF, other dynamic flip-flops employ structure to prevent the floating point. For example, Sdff [13] has a keeper at node X while HLFF [12], and CCFF [11] have a transistor connecting to Vdd when D=0, respectively. Both methods serve to increase noise robustness of node X.

Finally it is difficult to apply the low power techniques. For example, the clock structure with precharging transistors P1, P2 in CDMFF makes it difficult to apply double edge triggering. Nor can CDMFF be used in a low swing clock environment. (Note that the incoming low swing clock signal cannot drive pMOS, P1 and P2, in high voltage block (VDDH), because the pMOS transistors will not turn off by a low swing voltage, resulting in short circuit power consumption.)

clocked pre charging transistors (P1,P2) in CDMFF. Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors.

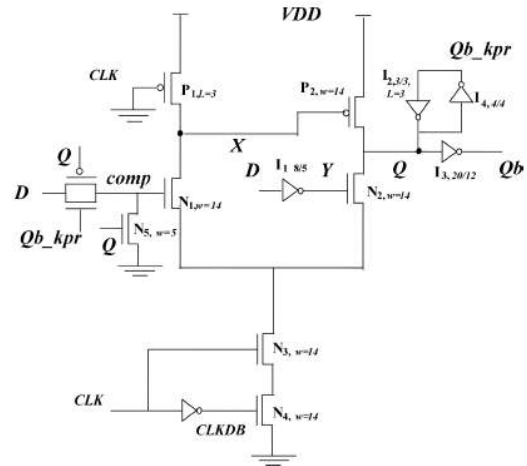


Fig.3.2. Clocked pair shared flip-flop.

#### IV. SOLUTION APPROACH

Around 66% of clock power is being dissipated in the last buffer stage driving the flip-flops leading to minor powersavings in LC globally-resonant [7] locally square CDNs. In order to achieve maximum power savings, the LC tank should drive the entire clock network without using intermediate buffers. This would require designing, modifying and understanding flip-flop performance with the sinusoidal clock signal generated in LC resonant networks, demonstrated that a low-swing square-wave clock double-edge triggered flip-flop[8] has enabled 78% power savings in the CDN [11]. The clock buffers are removed to allow the global and local clock energy to resonate between the inductor and entire clock capacitance including the receiving end flip-flops thus enabling maximum power savings. In addition, removing the clock buffers simplifies LC low-swing clocking [3] since only reduced swing buffers are used at the flip-flop gate and not in intermediate levels within the clock tree. A low swing differential conditional capturing flip-flop is used in low-swing LC resonant CDNs introduced, application of low-swing clocking to LC resonant CDNs. No additional power supply is required to achieve low-swing clocking.

A design of a global clock distribution network is presented in which four resonant circuits are connected to a conventional H-tree. Each quadrant consists of an on-chip spiral inductor that resonates with the wiring capacitance of the clock network and the decoupling capacitor is connected to the other end

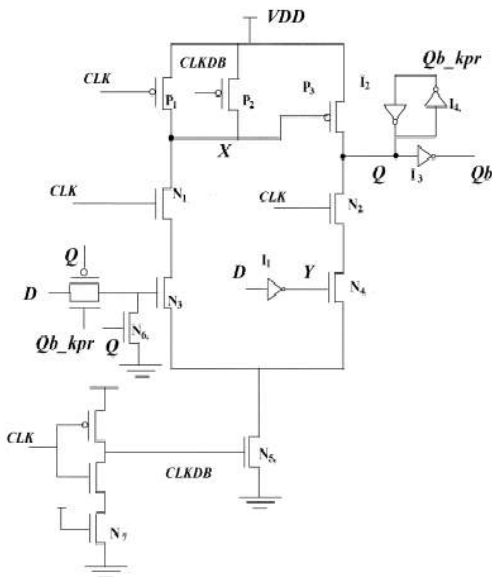


FIGURE 3.1: CDMFF

#### 3.5 CLOCKED PAIR SHARED FLIP FLOP (CPSFF)

Clocked Pair Shared flip-flop (CPSFF)[6] to use less clocked transistor than CDMFF and to overcome the floating problem in CDMFF as shown in fig 2.2. In the clocked-pair-shared flip-flop, clocked pair is shared by first and second stage. An always on p-MOS, P1, is used to charge the internal node rather than using the two



the full swing clock CLK\_FS and low swing clock signal CLK\_LS at the gate of transistor MN1 reaches 500 mV. At this point, node SET is pulled down and the output of the NAND latch is pulled up.

### V. CONCLUSION AND RESULT

Low swing differential capturing flip-flop (LSDCFF) consume less power. It reduces capacity of clock load, reduces Short circuit current power. Low swing differential capturing flipflop used only less clocked transistors, used less power. Overall power dissipation is different for the proposed methodologies due to the variation in the capacitive loading across the rotary ring. A novel energy recovery clocked flipflops that enable energy recovery from the clock network, resulting in significant total energy savings compared to the square-wave clocking. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency and implemented energy recovery clocked flipflops through a clock network driven by a resonant clock generator, generating a sinusoidal clock. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption. The power attained from low swing differential conditional capturing flip flop is 0.298mw.

The time delay in the clock unit can be reduced by minimizing the transistor count in that clock unit. In this way, the load seen by driving logic imposed by the flip flop is included in total power consumption. The performance simulations match the actual speed of the chip. Also, the global layout for the processor is a huge task, and the area optimizations at this top level will present the greatest gains towards a chip with a low area.

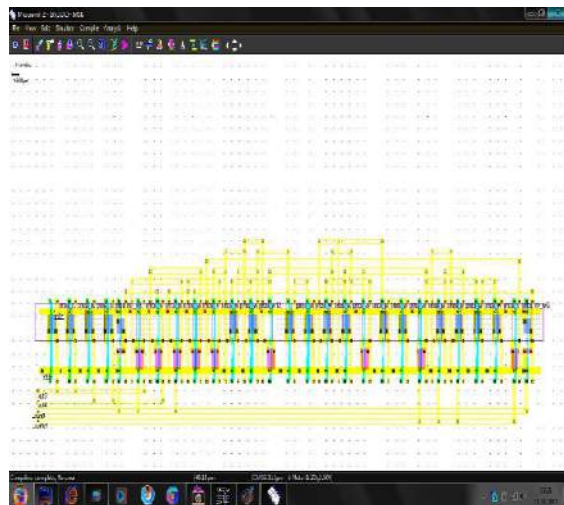


Fig.3. low swing differential conditional capturing flipflop layout diagram.

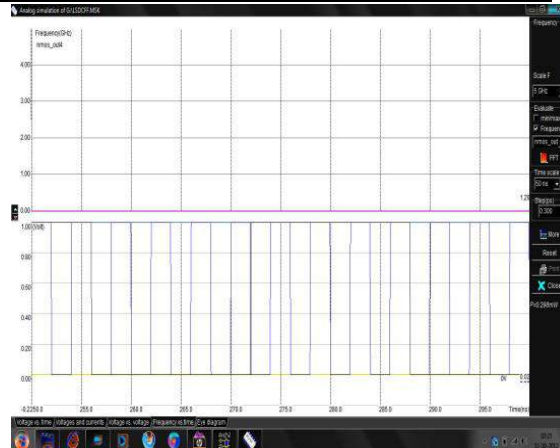


Fig. 4. frequency vs time graph

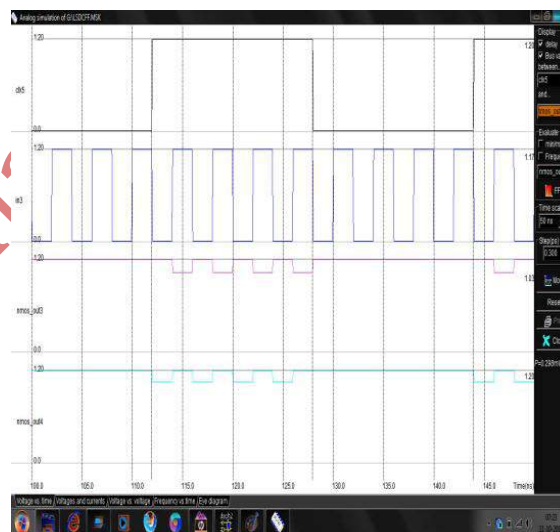


Fig. 5. voltage vs time graph

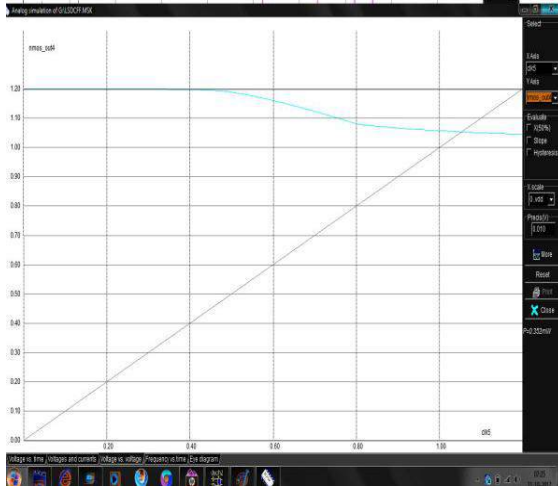


Fig.6. voltage vs current graph.

## APPLICATIONS:

- A flip-flop is essentially a 1-bit memory unit. Such memory units are highly useful in digital computers to store a binary number or to keep the information of previous counts and additions until these are needed.
- Memory circuits can be built using many flip-flops.
- Low Power Memory applications.

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## REFERENCES

- [1] C. J. Anderson, J. Petrovick, J. M. Keaty, J. Warnock, G. Nussbaum, J.M. Tendier, C. Carter, S. Chu, J. Clabes, J. Dilullo, P. Dudley, Harvey, B. Krauter, J. LeBlanc, L. Pong-Fei, B. McCredie, G. Plum P. J. Restle, S. Runyon, M. Scheuermann, S. Schmidt, J. Wagoner, R. Weiss, S. Weitzel, and B. Zoric, "Physical design of a fourth-generation POWER GHz microprocessor," in Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf., 2001
- [2] C. J. Anderson et al., "Physical design of a fourth-generation POWERGHz microprocessor," in IEEE ISSCC Dig. Tech. Papers, Feb. 2001
- [3] F. H. A. Asgari and M. Sachdev, "A low-power reduced swing global clocking methodology," IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol. 12, no. 5, pp. 538–545, May 2004.

[4] J. Clabes et al, "Design and implementation of the POWER5 microprocessor," in IEEE ISSCC Dig. Tech. Papers, Feb. 2004, pp.56–57.762

[5] A. J. Drake, K. J. Nowka, T. Y. Nguyen, J. L. Burns, and R. B. Brown, "Resonant clocking using distributed parasitic capacitance," IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1520–1528, Sep. 2004

[6] V. Gutnik and A. Chandrakasan, "Active GHz clock network using distributed PLLs," IEEE J. Solid-State Circuits, vol. 35, no. 11, pp.

[7] M. Hansson, B. Mesgarzadeh, and A. Alvandpour, "A 1.56 GHz on-chip resonant clocking in 130 nm CMOS," in Proc. IEEE Int. Custom Integrated Circuits Conf., 2003, pp. 241–244.

[8] C. Kim and S. M. Kang, "A low-swing clock double-edge triggered flipflop," in Proc. Symp. VLSI Circuits, 2001, pp. 183–186

[9] S. D. Naffziger and G. Hammond, "The implementation of the next generation 64 b Itanium™ microprocessor," in Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf., 2002, pp. 344–472.

[10] J. Pangjun and S. S. Sapatnekar, "Low-power clock distribution using multiple voltages and reduced swings," IEEE Trans.

[11] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock distribution networks in 3-D integrated systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 10.1109/TVLSI.2010.2073724.

[12] D. Pham et al., "The design and implementation of a first generation cell processor," in IEEE ISSCC Dig. Tech. Papers, Feb. 2005, pp.184–185.

[13] G. A. Pratt and J. Nguyen, "Distributed synchronous clocking," IEEE Trans. Parallel Distrib. Syst., vol. 6, no. 3, pp. 314–328, Mar. 1995.

[14] Z. Xu and K. L. Shepard, "Low-jitter active deskewing through injection-locked resonant clocking," in Proc. IEEE Int. Custom Integrated Circuits Conf. (CICC), 2007, pp. 9–12.