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Design of Low Power Digital Barrel Shifter Data path Circuit

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ABSTRACT

In Standard Cell Based Design, the cells are placed together in rows but there is generally no regularity to the arrangement of the cells within the rows, the software used arrange the cells and complete the interconnect. In Datapath automatically takes care of most of the interconnect between the cells with regular layout, which produces predictable and equal delay for each bit, Interconnect between cells can be built into each cell. In today's electronic gadgets, there is a need for low power digital VLSI design as the performance of portable electronic products increases continuously with demand, Due to usage of batteries, the operating time of portable electronic products is prime factor. In this project we implement Multiplexers using Conventional style and Transmission gate logic, 4 bit barrel shifter, voter circuit using 2-1 multiplexers and Barrel shifter with a voter circuit, the voter circuit here is the datapath circuit. The simulations are performed on various foundry technologies and the one with low power dissipation is proposed.

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Keywords: Barrel shifter, low power, voter circuits, transmission gates, Multiplexer.

1. INTRODUCTION:

We solicit that barrel shifters are math and rationale circuits that might make used on movement or turn information in a universally useful chip or advanced sign processor. An barrel shifter principally offers five operations; turn right, turn left, shift right logical, shift cleared out logical, What's more movement correct math.

Operations

An barrel shifter principally offers five operations; turn right, turn left, shift good logical, movement exited logical, and movement straight math. Occasionally, those movement cleared out number-crunching operation is likewise included, at it is not backed in the outlines nitty gritty here because of its rare utilization..

Rotate:

An turn is a cyclic movement possibly of the left alternately right. This implies that concerning illustration odds are moved out of the information vector for you quit offering on that one side, they are moved under the information vector on the different side. Throughout this process, the sum odds from those information need aid routed of the yield. Their position in the output, however, will be not so much those same Likewise it might have been in the enter.

Concerning illustration indicated to figure 1. a, a k-bit turn straight moves k low request odds of the vast majority huge limit of the touch vector. Likewise, Similarly as indicated for figure 1. b, a k-bit turn exited moves k secondary request odds of the slightest huge end of the bit vector. Those remaining (n-k) odds are moved Along these lines Likewise on fill the void cleared out Toward the k odds moved Previously, an cyclic way..

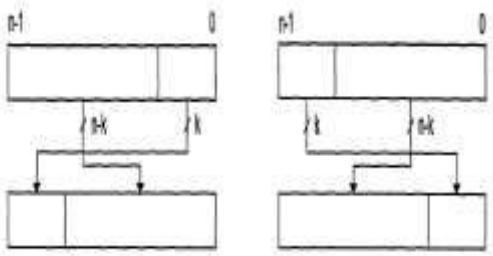

Figure1a, b: Rotate Right, Rotate left

A sample of the turn correct could a chance to be seen Previously, figure 2 the place a 32-bit expression about information need a low request byte turned good. As could a chance to be seen, this byte may be moved under the A large portion huge parcel of the saying. Those remaining odds are basically moved of the straight. This fills those void left Eventually Tom's perusing the byte moved and at the same time makes a void in the helter skelter request touch district to the turned byte to make put. In An comparable fashion, figure 3 shows the way to which a secondary request byte may be moved under the low request locale of the expressions Throughout a turn exited. Over both instances, a byte for information may be moved starting with one limit of the statement of the different with whatever remains of the statement reorienting itself to suit this change.

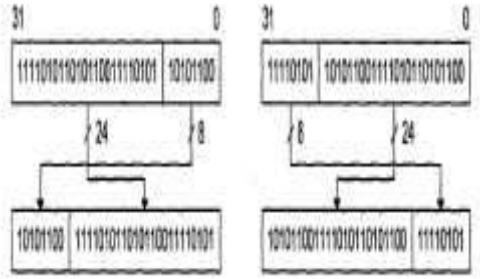

Figure2: Rotate right left example

Shift Right Logical

Those movement straight intelligent operation is a great deal in An turn right, Anyhow without those k low request odds being moved should a secondary request position. Instead, the low request odds need aid uprooted. The remaining (n-k) odds would moved of the right with the goal Similarly as to fill those void made by those misfortune of the low request odds. Those void made in the helter skelter request locale Toward this movement is filled with zeros.

The void made in the helter skelter request locale by this movement will be loaded for zeros. Figure 4 illustrates this procedure and figure 5 will be a sample of a shift straight legitimate Eventually Tom's perusing 8 operations.

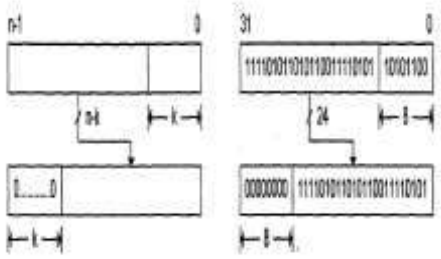

Figure3: Shift right logical

Those shift exited intelligent operation is comparative of the shift correct intelligent operation. Those difference, for course, lies in the course of the shift, which, in this case, will be of the cleared out. Concerning illustration such, those k helter skelter request odds are evacuated from

those secondary request locale so that the remaining (n-k) odds might a chance to be moved of the left k puts.

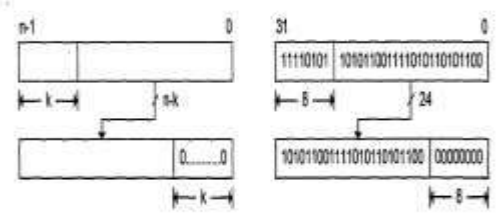

Figure 4: Shift left logical

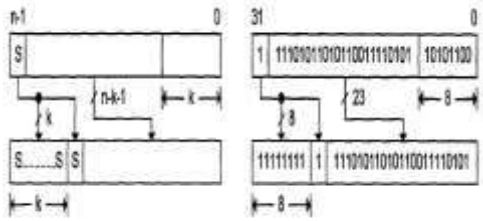

Figure 5: Shift right arithmetic

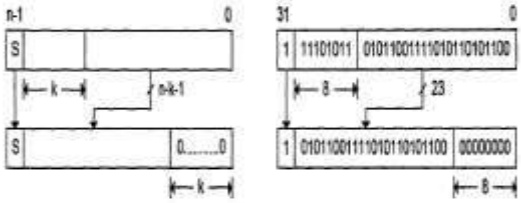

Figure 6: Shift left arithmetic

2. IMPLEMENTAION:

Barrel shifters often prepare flags that show uncommon states. The two practically regular are those zero What's more flood flags. Those zero banner will be a basic I-bit banner that demonstrates if those consequence of the operation performed need An quality from claiming zero. An worth from claiming one demonstrates that the bring about shortages is zero, same time An zero demonstrates a non-zero consequence. This banner may be functional At the effect is utilized within an correspondence test with zero, Likewise is done in a portion processors, or The point when those result of a shift/rotate operation sets those processor state codes. Those flood banner may be Additionally An I-bit banner. It will be used to demonstrate a sign spot progress Throughout a left shift operation. A greater amount specifically, On those shift were on be actualized Concerning illustration progressive I-bit shifts, afterward flood may be said will happen On In any side of the point Throughout the process, those touch death over those sign spot area may be not the same as the unique sign spot. Flood may be shown by An worth for one. The flood banner may be functional when you quit offering on that one needs should think On the genuine outcome can't be spoke to utilizing n odds.

3. TMR

TMR is one of the solutions to make a circuit be able to tolerate occurrence of an error and correct it. Basically, a TMR system is composed of three identical devices and voting logic ragged.

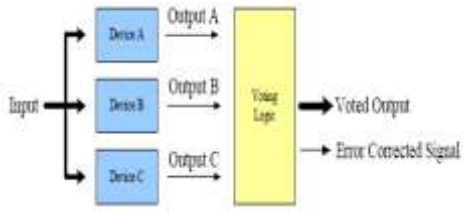

Figure7: Basic TMR Concept

Table 1. Power consumption

Technology	No.of Metals	Vdd(V)	Power dissipation
120 nmt	6	1.20-2.50	0.231mW
90nmt	6	1.00-2.50	0.170mW
70nmt	6	0.7-2.50	51.192µW
50nmt	7	0.5-2.50	12.720µW

4. FIGURES/CAPTIONS:

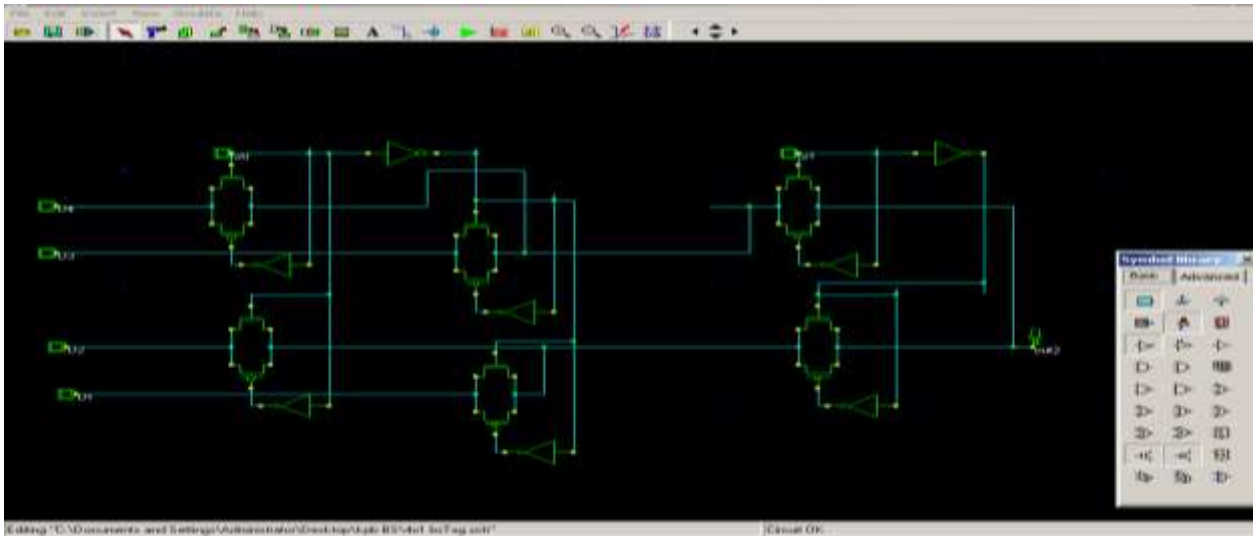

Fig 8: 4x1 mux using Tx gates

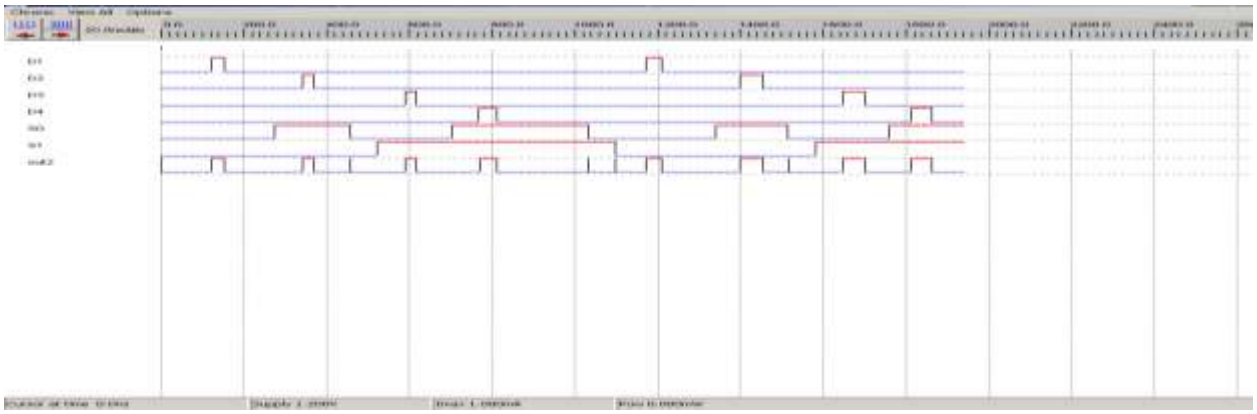

Fig 9: 4x1 mux using Tx gates simulation using DSCH

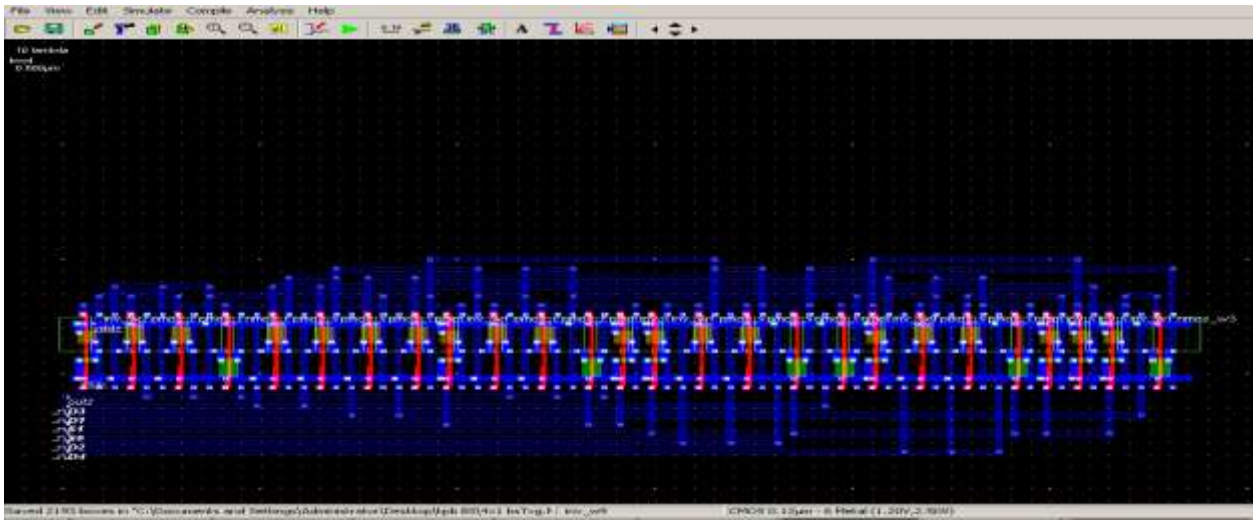

Fig 10: 4x1 mux using Tx gates Layout

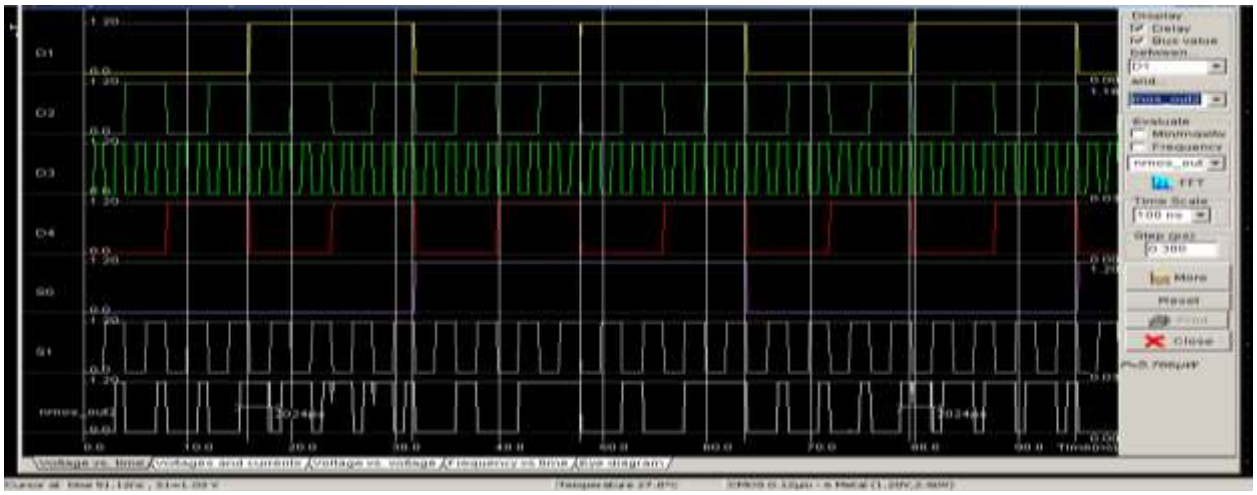

Fig 11: 4x1 mux using Tx gates Analog simulation

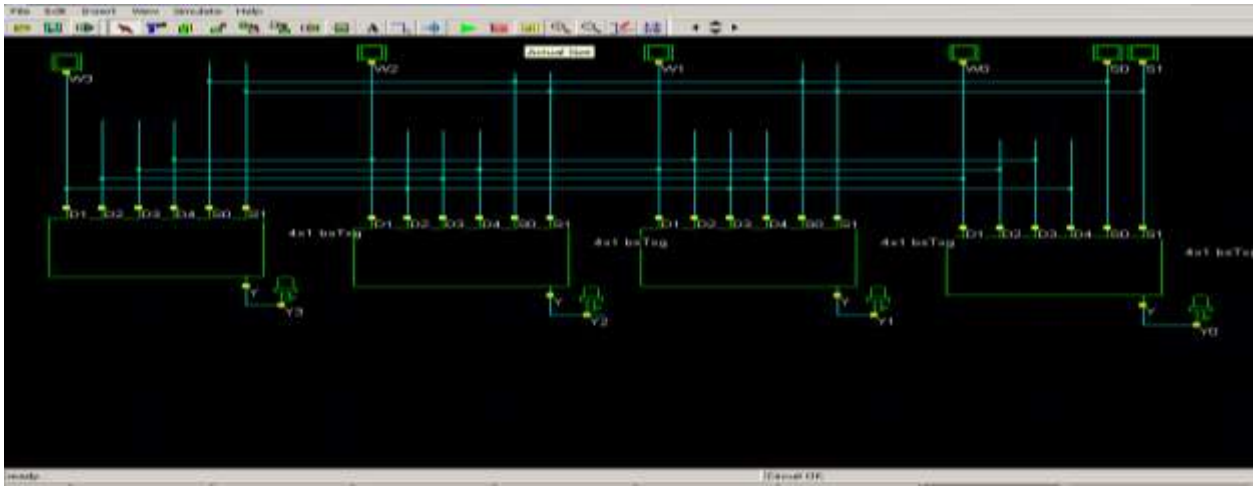

Fig 12: 4x1 barrel shifter

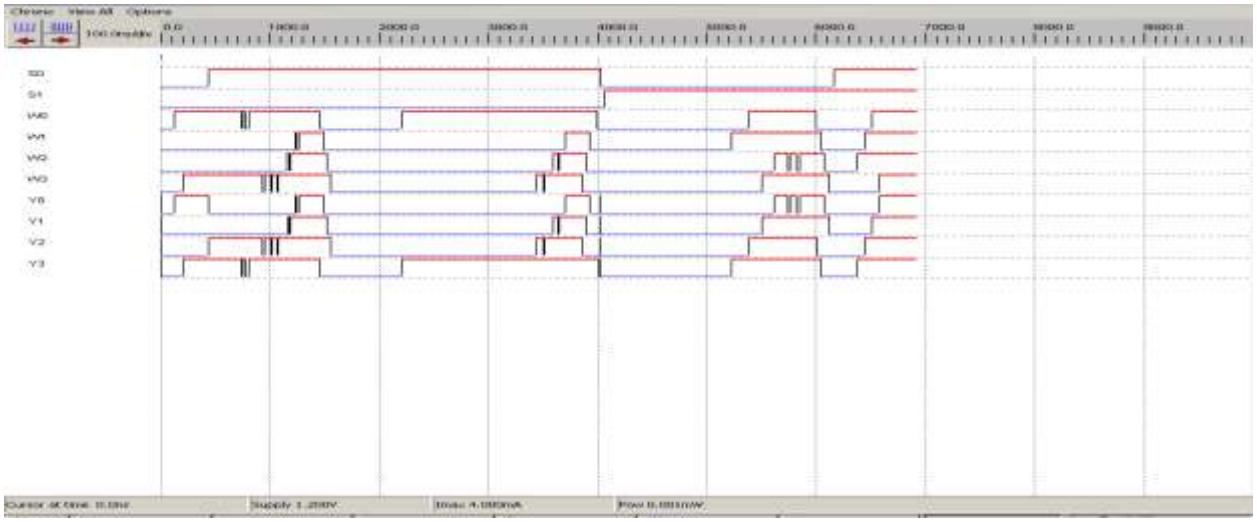

Fig 13: barrel shifter simulation using DSCH

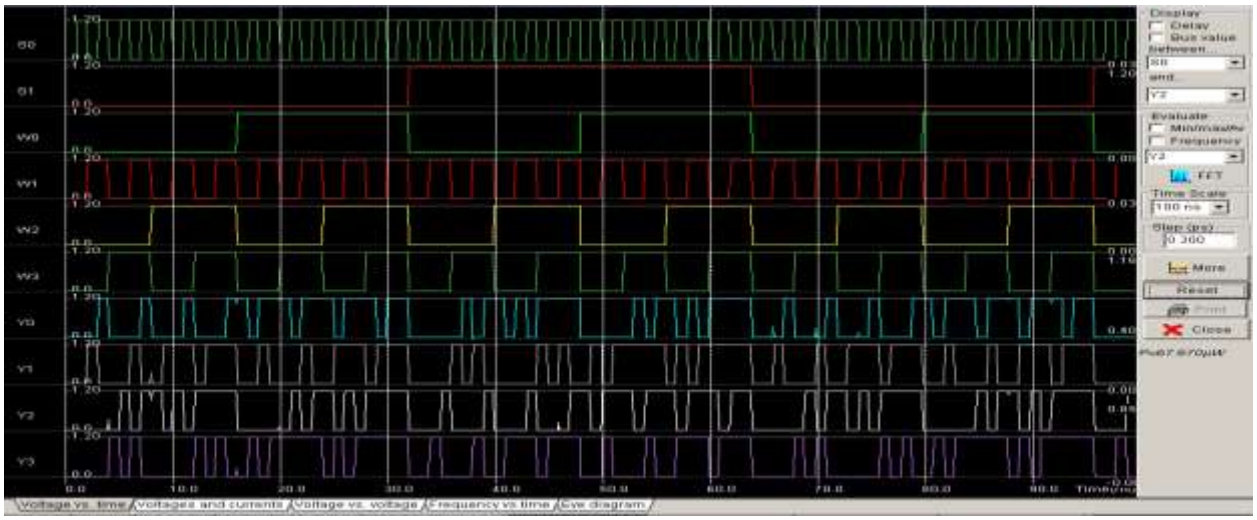

Fig 14: barrel shifter Analog simulation

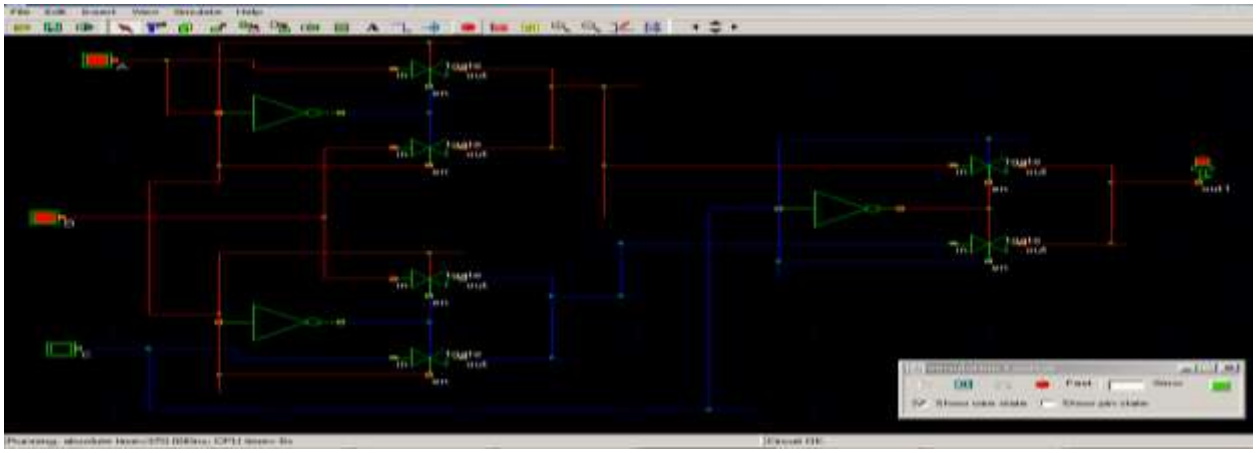

Fig 15: Voter Circuit

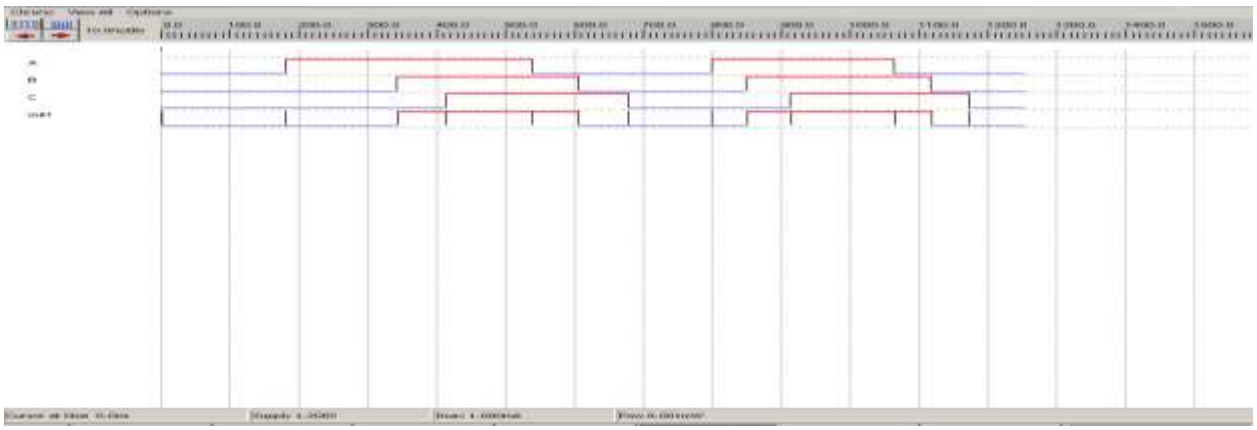

Fig 16: Voter Circuit simulation using DSCH

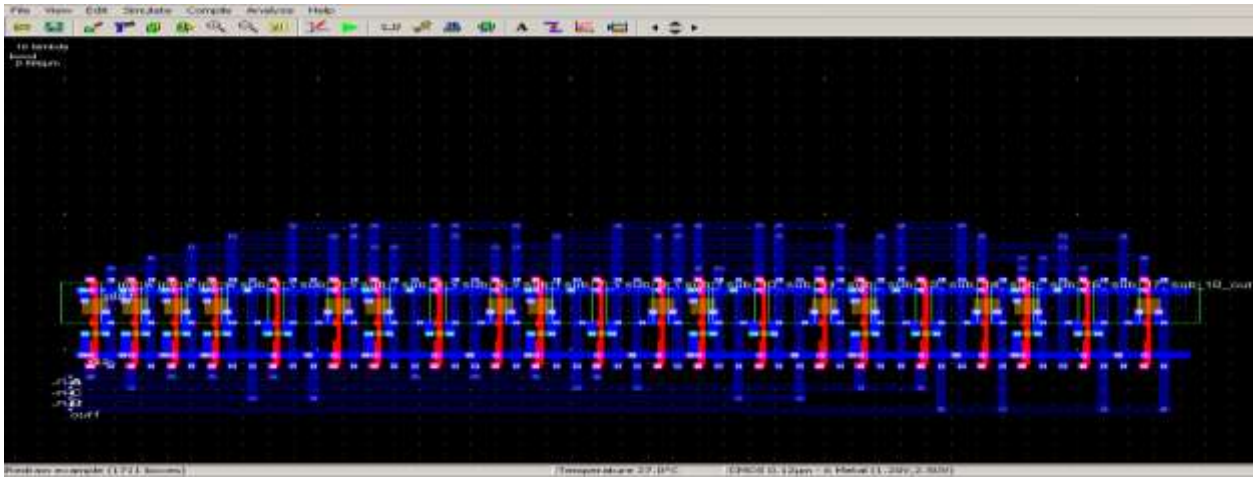

Fig 17: Voter Circuit Layout

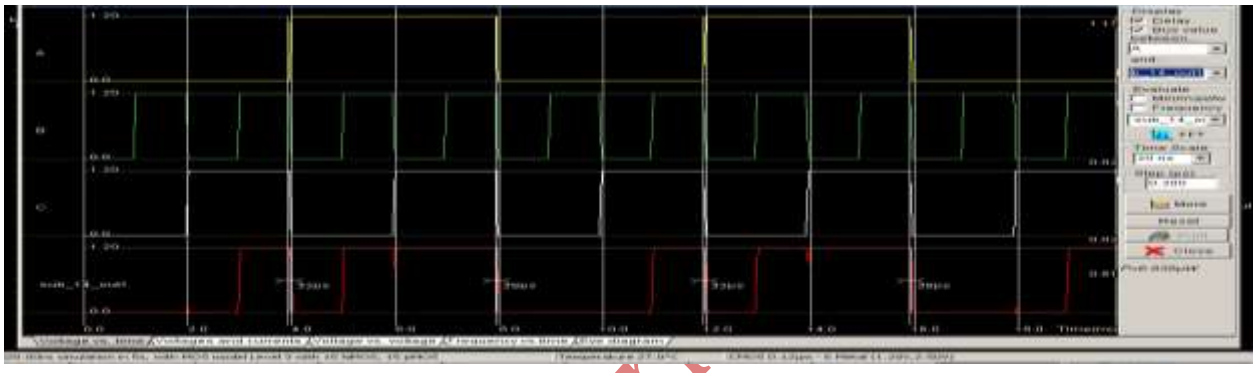

Fig 18: Voter Circuit Analog simulation

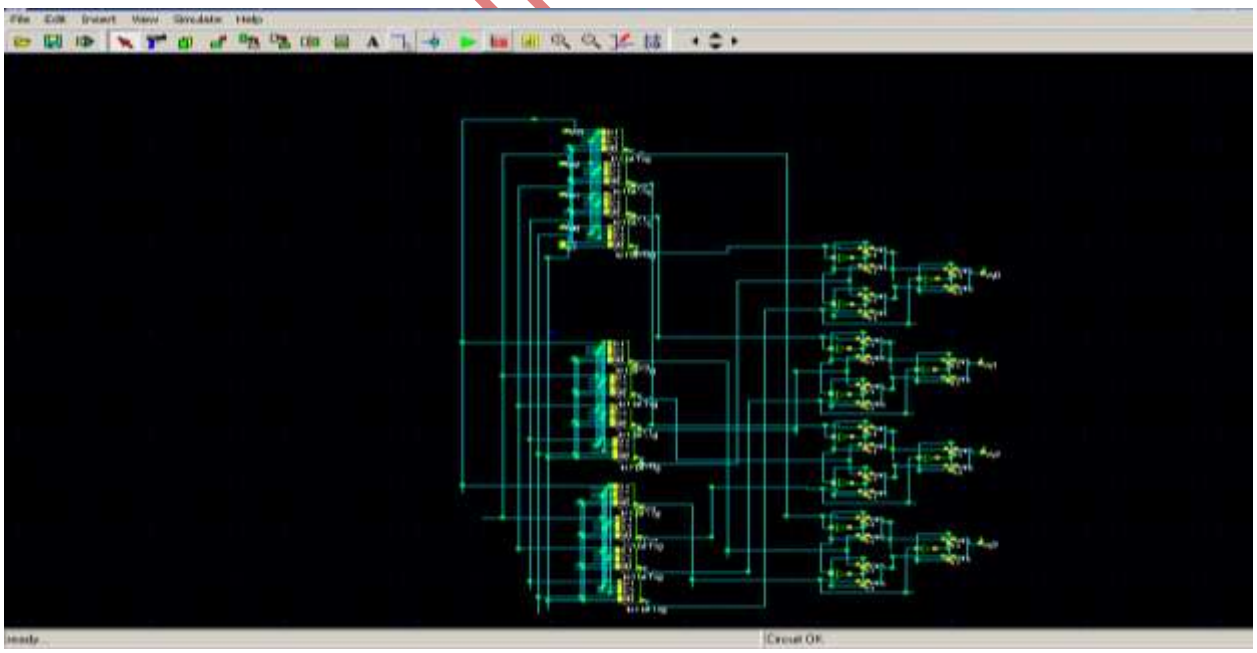

Fig 19: Barrel shifter with a proposed voter circuit

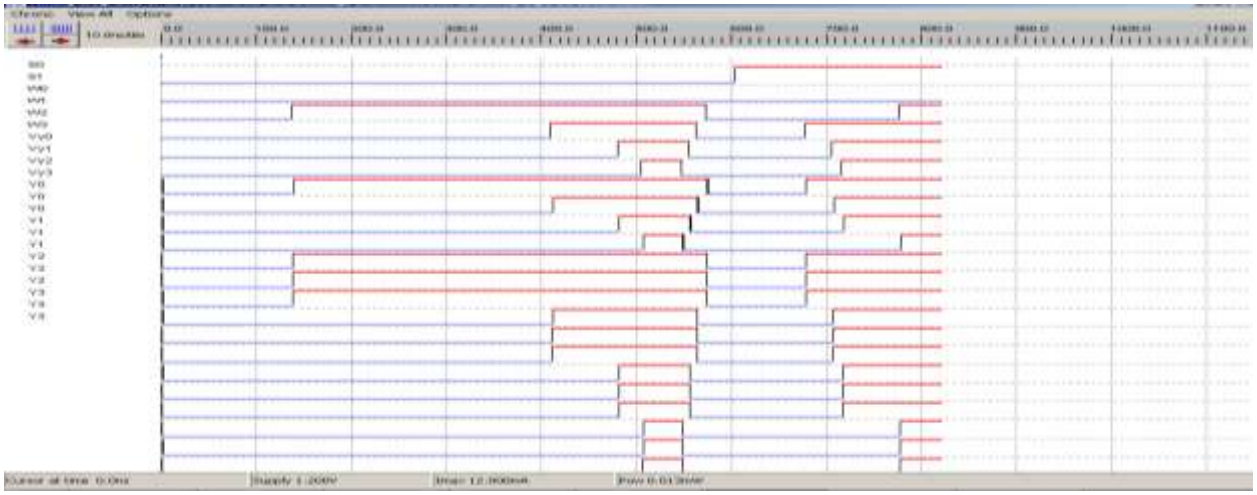

Fig 20: Barrel shifter simulation using DSCH

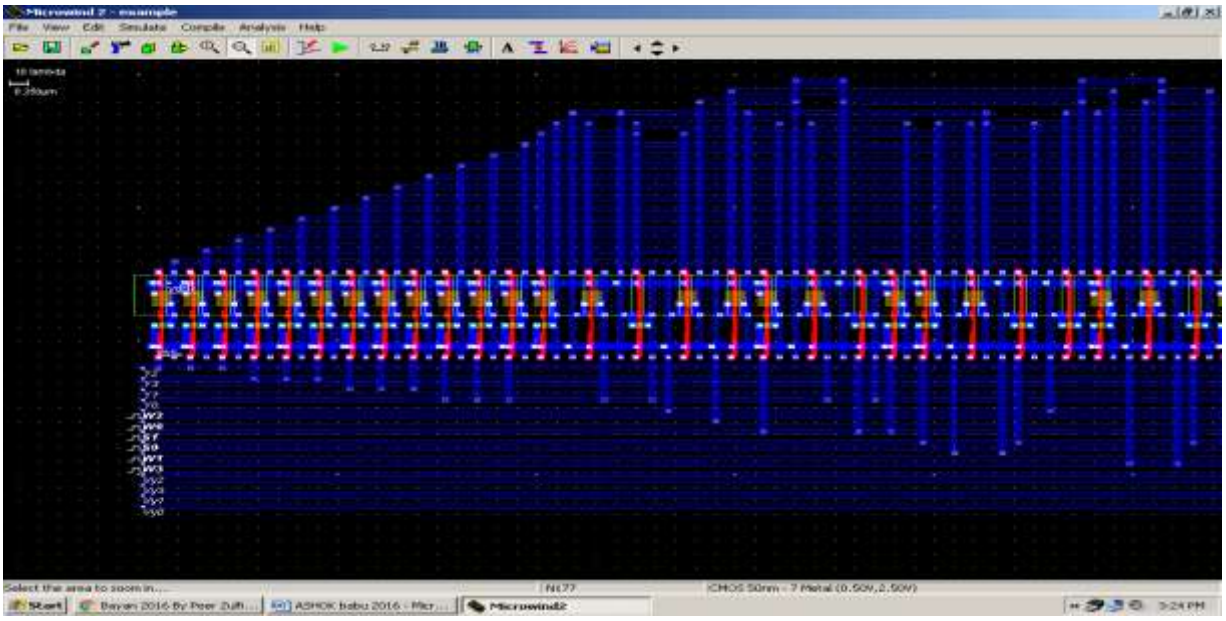

Fig 21: Barrel shifter Layout

Fig 22: barrel shifter Analog simulation 120 nmt technology

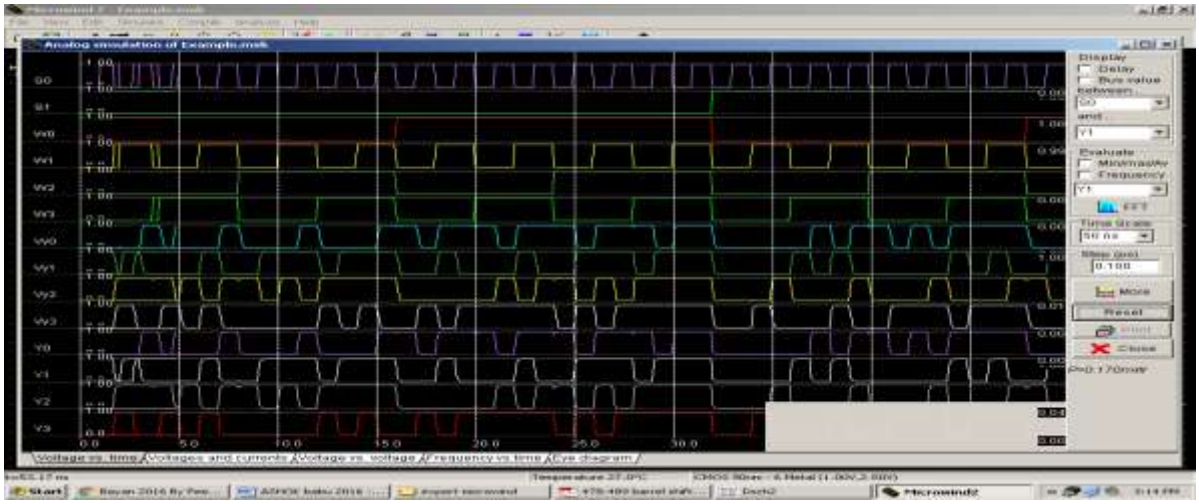

Fig 23: barrel shifter Analog simulation in 90 nmt technology

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