

# High Speed, Low power 70nm Double Tail Comparator

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## ABSTRACT

*In the latest technological invention of ultra high speed and low power analog to digital converters Comparator is the most important section. In this paper analysis of operating frequency and power consumption of double tail dynamic comparator is presented. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages without complicating the design. Simulation results in a 70nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.94 GHz at supply voltages of 1 V, while consuming .18mW, respectively. By adding some transistor and by changing the physical specification of transistor. By doing this we achieved improved characteristics of double tail dynamic comparator.*

**Keywords:** Comparator, Double-tail comparator, 70nm.

## 1. INTRODUCTION

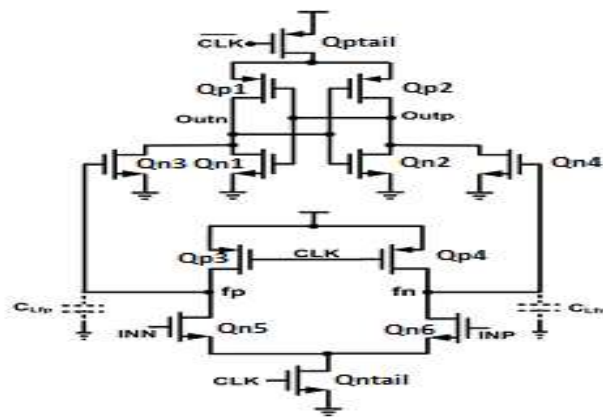
The comparator circuit is one to which a linear input voltage is compared to another reference voltage, the output being a digital condition representing whether the input voltage exceeded the reference voltage. Many high-speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. In general comparators are “fast”. The circuits of comparators are not immune to speed power trade off. High speed comparators such as flash ADC’s use

transistors with large aspect ratios and hence also consume more power. So depending on the application a comparator with either high speed or low power should be selected. Nano scale comparators are ideal for portable and ultra-low-power applications. Lower power and Good accuracy can be obtained by using a clocked comparator structure. This clocked comparator structure, when the clock is high, uses strong positive feedback for a “Regenerator phase” and enters into a “Reset phase” when the clock is low. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures.

In this paper, a comprehensive analysis on delay, power consumption and area of the dynamic comparator with different architecture will be presented. Based on the double tail structure of 70 nm, proposed comparator is designed which does not require stacking of too many transistors. By using power gating technique and by adding few minimum size transistors to the conventional double tail comparator, latch delay and power consumption



During reset phase ( $CLK=0$ ,  $Q_{ntail}$ , and  $Q_{ptail}$  are off), transistors  $Q_{P3}$ - $Q_{P4}$  pre-charge  $f_n$  and  $f_p$  nodes to  $V_{DD}$ , which in turn causes transistors  $Q_{N3}$  and  $Q_{N4}$  to discharge the output nodes to ground. During decision-making phase ( $CLK = V_{DD}$ ,  $Q_{ntail}$  and  $Q_{ptail}$  turn on),  $Q_{P3}$ - $Q_{P4}$  turn off and voltages at nodes  $f_n$  and  $f_p$  start to drop with the rate defined by  $I_{Q_{ntail}}/C_{fn}(p)$  and on top of this, an input-dependent differential voltage  $V_{fn}(p)$  will build up. The intermediate stage formed by  $Q_{N3}$  and  $Q_{N4}$  passes  $V_{fn}(p)$  to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.



**Fig 2: Conventional double-tail dynamic comparator.**

Some important notes can be concluded from study of double tail dynamic comparator.

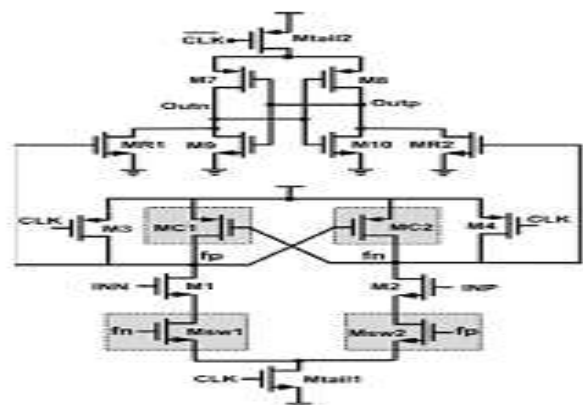
The voltage difference at the first stage outputs ( $V_{fn}/f_p$ ) at time  $t_0$  has a profound effect on latch initial differential output voltage ( $V_0$ ) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.

In this comparator, both intermediate stage transistors will be finally cut-off, (since  $f_n$  and  $f_p$  nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to  $V_{DD}$ , which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

### 2.3 Comparator Designed by Samaneh Babayan Mashhadi

In this dynamic comparator two control transistors ( $M_{c1}$  and  $M_{c2}$ ) have been added to the first stage in parallel to  $M_3/M_4$  transistors but in a cross-coupled manner to increase  $V_{fn}/f_p$  in order to increase the latch regeneration speed. During reset phase ( $CLK=0$ ,  $M_{tail}$  and  $M_{tail2}$  are off, avoiding static power),  $M_3$  and  $M_4$  pulls both  $f_n$  and  $f_p$  nodes to  $V_{DD}$ , hence transistor  $M_{c1}$  and  $M_{c2}$  are cut off. Intermediate stage transistors,  $M_{R1}$  and  $M_{R2}$ , reset both latch outputs to ground.

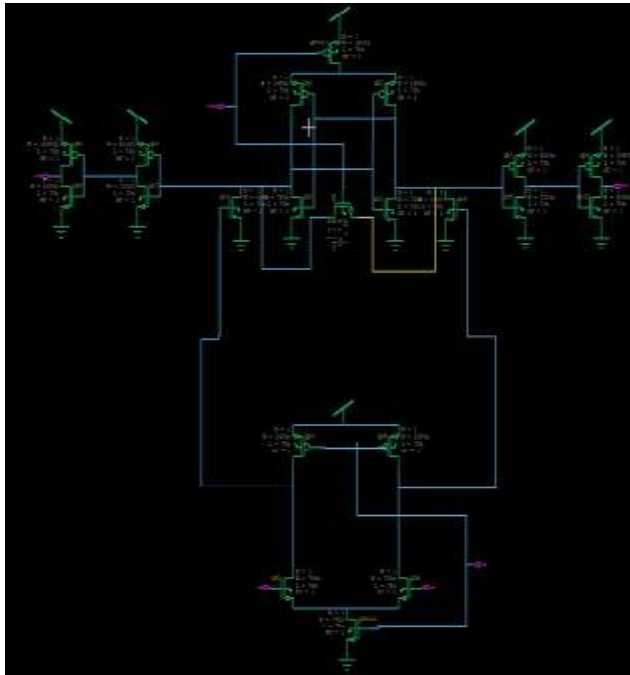
During decision-making phase ( $CLK=V_{DD}$ ,  $M_{tail1}$ , and  $M_{tail2}$  are on), transistors  $M_3$  and  $M_4$  turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since  $f_n$  and  $f_p$  are about  $V_{DD}$ ). Thus,  $f_n$  and  $f_p$  start to drop with different rates according to the input voltages. Suppose  $V_{INP} > V_{INN}$ , thus  $f_n$  drops faster than  $f_p$ , (since  $M_2$  provides more current than  $M_1$ ). As long as  $f_n$  continues falling, the corresponding pMOS control transistor ( $M_{c1}$  in this case) starts to turn on, pulling  $f_p$  node back to the  $V_{DD}$ ; so another control transistor ( $M_{c2}$ ) remains off, allowing  $f_n$  to be discharged completely. By the time passing, the difference between  $f_n$  and  $f_p$  ( $V_{fn}/f_p$ ) increases in an exponential manner, leading to the reduction of latch regeneration time. In this circuit, when one of the control transistors (e.g.,  $M_{c1}$ ) turns on, a current from  $V_{DD}$  is drawn to the ground via input and tail transistor (e.g.,  $M_{c1}$ ,  $M_1$ , and  $M_{tail1}$ ), resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistors [ $M_{sw1}$  and  $M_{sw2}$ ].



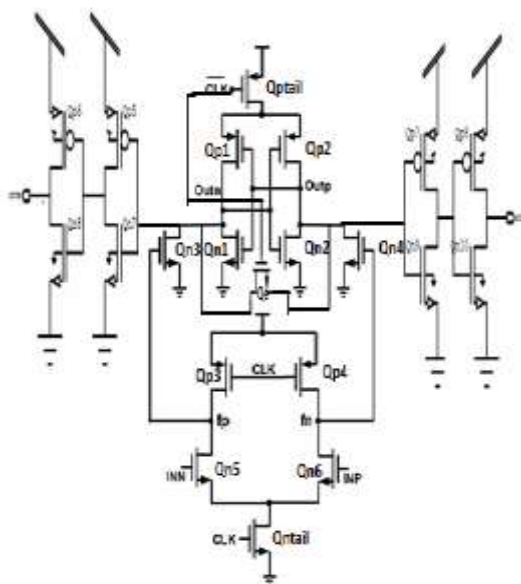
**Fig 3: Mashhadi's Comparator**

### 3. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

The proposed double-tail dynamic comparator is made on 70nm scale. A change in the design of conventional dynamic comparator is done in decision making portion. The proposed design is shown in fig 4.



(a) Schematic view



(b) Simplified schematic view

Fig 4: Proposed double-tail dynamic comparator.

Operation of proposed comparator - The operation of proposed comparator as follows. During the reset phase (CLK = 0, Qptail and Qntail are off, avoiding static power), Qp3 and Qp4 pulls both fp and fn nodes to Vdd. Intermediate stage transistors Qn3 and Qn4 reset both latch output to ground. During the decision making phase (CLK = Vdd, Qptail and Qntail are on), transistor Qp3 and Qp4 turns off. Furthermore at the beginning of this phase the control transistors are still off (since fn and fp are about Vdd). Thus fn and fp starts to drop with different rates according to the input voltages. Suppose  $V_{inp} > V_{inn}$ , thus fn drops faster than fp.(since Qn6 provides more current than Qn5). According to that Qn3 and Qn4 reacts which goes high for 0 input, and allows the input to flow in form of 0 or 1 from any of the output either from outn or outp As per the output we get to know which kind of signal we are getting either it is input or reference. The proposed design consist three designing change in conventional double tail comparator, one of which is NMOS transistor Qe which is on for clock input 1 and other change is at the output portion which is addition of two inverter on either side of output in form of Qp5-Qn7, Qp6-Qn8 at outn node and pair of Qp7-Qn9, Qp9-Qn10 at outp side. And the third and important change is that comparator is made on scale of 70 nm length, which reduces its transistor length less than half of the length used in base paper design. These changes are having their own importance in circuit to improve some of the characteristics.

As the size of transistor is reduced to 70nm that will reduce the size of comparator on chip. Reduction of size definitely advantage for reduced size chips and which makes a designer capable to put more devices on a single chip but it also comes with some of disadvantages which need to be compensated by some mean. In this circuit because of the reduced size of transistors we are not able to drive the circuit on 0.8V voltage as the previous comparator was working but still we are able to drive the circuit on 1V which is already in range of our previous circuit. To achieve a reduced time and low power operation we have used additional transistors like Qe and pair or two inverters on each output. The effect of these additional transistors is as follows.

### 3.1 Effect of Qe in proposed comparator design

The Qe is most important designing advantage in the circuit. We will see below how the circuit will work with or without Qe. A NMOS transistor is used as Qe which is ON for 1 and OFF for 0 input. So whenever circuit is in precharge phase the Qe transistor is in operation and when comparator is in decision making phase Qe is not in operation or it is in off condition because it is directly connected with clock bar. Let consider a case  $I_{nn} > I_{np}$  in this case when clock input is rising or going from 0 to 1 or it is in decision making phase both outp and outn rises but because outp is strong it reaches to 1 and outn again reaches to 0. When clock reaches from 1 to 0 outp also starts to decay and outn already in 0 conditions because for comparison both the input should be on equipotential and because of this comparison will again start from 0V. In this case until both input reaches to 0 comparison is not possible which consumes time and power.

To avoid this condition Qe is used which work in the pre charge phase. This is the phase when outp is in exponential decay condition and reaches to 0. In the precharge phase clock is 0 and because of that Qptail and Qntail is off and circuit doesn't make any decision. In precharge phase Qe starts and try to pull both the input on equal potential. Let outp is decaying and outn is on 0V so Qe shorts both the inputs and try to pull outp down towards 0V and try to pull outn upwards towards 1 volt because of shorting outp and outn reaches to equal potential at somewhere in middle and from there again comparison starts. Which saves clock and power and results fast speed and low power circuit.

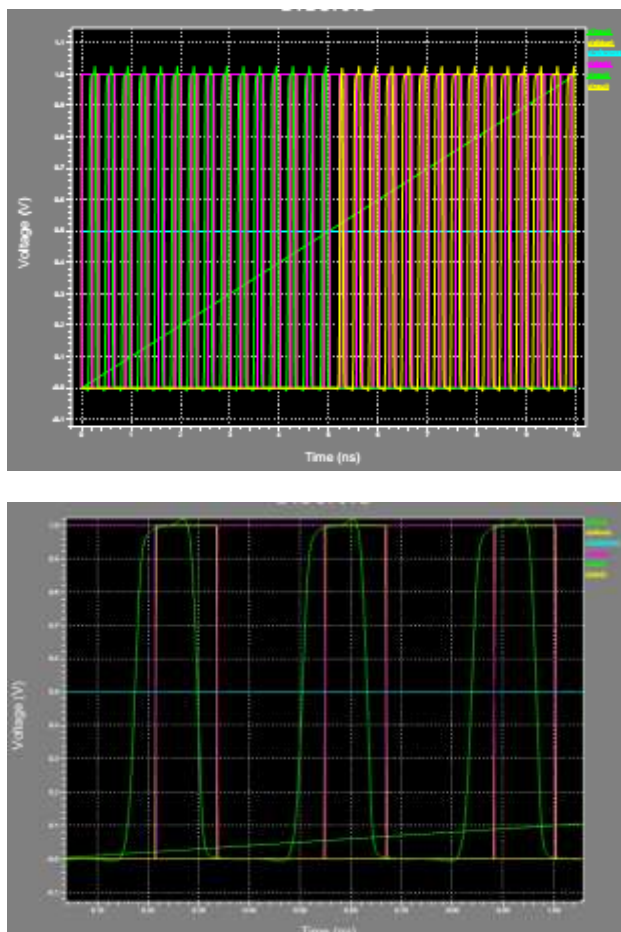
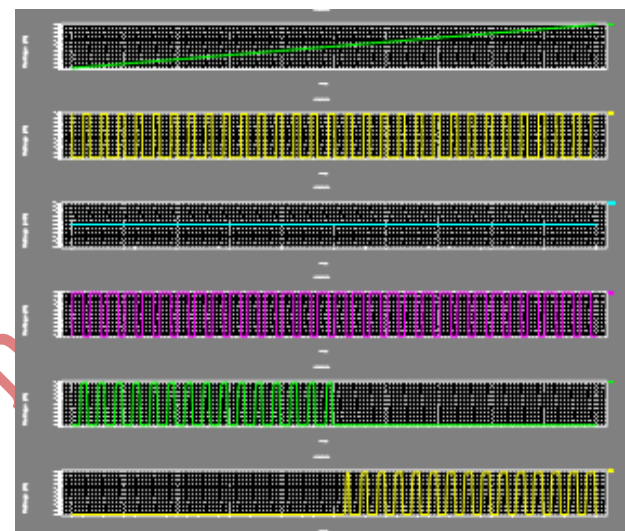


Fig. 5: Full circuit waveforms



### 3.2 Effect of pair of inverters at the output

The set of inverters is being used at the output of circuit before outp and outn nodes these inverter works as post amplifiers circuit. The post amplifiers are being used at the output node which can give amplifies current or power for the further circuit which will be connected to the comparator's output node. If the comparator is providing low power the post amplifier compensate the power and provide appropriate drawing power to the output. Here each preceding post amplifier is three times of its previous amplifier. We can add more post amplifiers as per our requirement.

## 4. DESIGN CONSIDERATION

In designing the proposed comparator some design issue must be consider as the circuit is made with 70nm scale for that the input voltage range is increased and for proper operation of circuit as well

as circuits connected with this additional transistor are given.

### 5. SIMULATION RESULT

The proposed comparator is simulated and compared with conventional double tail comparator and the base paper comparator we found following results that preceding circuits simulated in .18-um CMOS technology with Vdd 1.2V but this circuit is designed in 70nm CMOS technology with Vdd 1V. Where because of  $Q_e$  in the circuit the exponential time decay is improved. The isolating transistors  $Q_{n3}$  and  $Q_{n4}$  works as isolators between pre charge phase and decision making phase. This isolating transistor also works as kickback noise reduction component and provides positive feedback.

Speed can be calculated by time which is taken by circuit for completing one cycle. As it is taking less than .34ns so

$$f = 1/t$$

$$f = 2.94 \text{ GHz and}$$

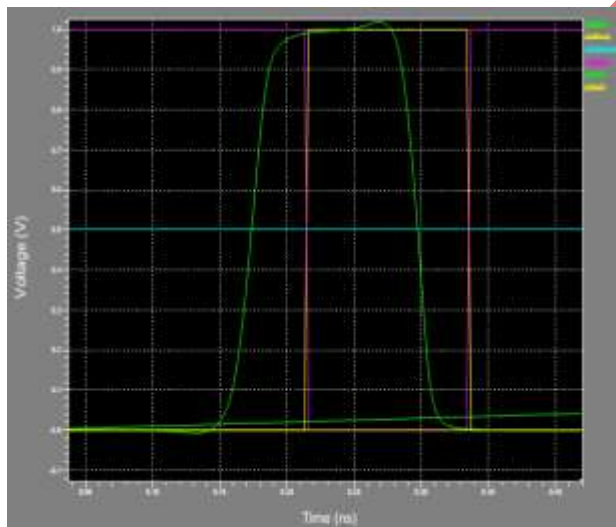


Fig 6: One cycle completion.

Power can be calculated by

$$P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T P(t) dt$$

$$\text{By that } E = P * T = .18pJ.$$

Table 1.Summary of the comparator performance

Item	Value
Technology	70nm CMOS
Supply voltage	1V
Operating frequency	2.94 GHz
Energy per conversion	.18pj

Table 2.Performance Comparison

Comparator Structure	Conventional dynamic comparator	Double-tail comparator	Mashhadi's comparator	Proposed dynamic comparator
Technology CMOS	180nm	180nm	180nm	70nm
Supply voltage	0.8V	0.8V	0.8V	1V
Maximum sampling frequency	900Mhz	1.8Ghz	2.4Ghz	2.94Ghz
Energy per conversion	0.3pJ	.27pJ	.24pJ	.18pJ

### 6. CONCLUSION

In this paper we presented a double tail dynamic comparator made with 70nm CMOS technology and which is compared with conventional dynamic comparator and two double tail dynamic comparator which were simulated on 180nm technology. Based on theoretical analysis we designed our comparator and derived improved results in form of operating frequency reduced energy consumption per conversion which is reduced up to great extent in proposed comparator.

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