ijournals International Journal of Software & Hardware Research in Engineering
ISSN No: 2347-4890 Volume 2 Issue 2, February 2014

# Reducing Power In Glitch Free Universal Gate Using Dcdl Technique

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## ABSTRACT

In this paper by using logical gates reducing delay produced by the output of circuit. Many circuits designed having glitching problem which have been used in many application. To overcome this glitching problem in the circuit universal circuits have been used. The NAND and NOR gate have been used and power consumption of circuit also reduced from micro watt to Nano watt. Control bits used in the circuit also minimizes the delay. Delay cells are used to control the glitching problem; these cells are controlled in digital manner. Digital to analog converters have been used to analog signals. It has been used in many applications. Resolution of circuit is maintained and power consumption is reduced. It can also reduce the crosstalk present in the signals and also minimizes the delay of the circuit. Power consumption of circuit using NOR gate is less than the circuit constructed using NAND gate.

## General Terms

All digital delay locked loop, delay cell, phase locked loop, digitally controlled delay line.

## Keywords

Reducing power, removing glitch, logical gates.

## 1. INTRODUCTION

The basic aim of this paper is to avoid glitches present in the circuit which is constructed using universal gate. Power is also analyzed to maintain low power consumption. Many methods are used to remove glitches present in the circuit. Delay have been reduced by using delay cell in each element of circuit and power consumption also reduced by microwind technology. Presence of glitch may cause unwanted transition in the circuit result. Jitter also cause undesirable deviation of periodic signal it may also results glitches in the circuit.
Jitter may be caused by interference of the signal and crosstalk with carriers of other signals.

Digital to analog converters or analog to digital converters used and time between samples varies. Time resolution of digital signal is higher than the voltage resolution of analog signal. Digitally controlled delay technique plays a role in analog to digital converters in circuit. In each element of circuit delay cell is constructed to reduce the output delay. A delay element is discrete element which allows signal to be delayed number of samples.

Power consumption of both NAND and NOR circuit is analyzed and it is less existing NAND based circuit. Minimizing the delay of circuit depends on the number of delay. Output capacitance and drivability of delay elements are the key parameters for designing low jitter delay elements. Each circuit can be constructed using NAND and NOR gate maintain same resolution with minimum delay produced. Delay element constructed using regular cascade of cells. It has simple layout organization with low nonlinearity effects. Hence removal of glitch in circuit and low power consumption of universal circuit has proposed in this paper.

## 2. RELATED WORKS

2.1) A portable Digitally Controlled Oscillator Using Novel Varactor.

A portable digitally controlled oscillator by two input NOR gate as a digitally controlled varactor in fine tuning delay cell design. It uses gate capacitance under different digital control inputs with delay resolution 256 times better than single resolution time. Phase locked loop used in many communication systems to clock and data recovery or frequency synthesis. To process high resolution digitally controlled oscillator by using NAND /NOR gate as novel varactor. Resolution is non-uniform and sensitive to power supply variation. It has high portability and short design turnaround cycle and also have small size of varactor. The driving strength can be changed by using capacitance loading.



 

2.2) Low Cost Variable Delay Line for Impulse Radio Ultra Wide Band Architecture.

It introduces delay line circuit suitable for impulse radio ultra wideband architecture. Fine synchronization used to be related to relative high cost devices. Low power architecture has been tested by commercial off the shelf breadboard. This achieves good performance and delay step in nanosecond range. Its band width is greater than 0.25MHz which is more than radiated spectrum. Additional circuit is needed to perform full clock cycle. Reference voltage can be adjusted with digital to analog converter. High data rate and low power system of wireless networking developed by using local area networking. This technique is based on broadcasting of very low power signals. Simple hardware is added to reduce latency. Delay is up to 40% of pulse width. Incoming signal delay depends on threshold voltage. Design is simple and fast circuit implementation.

2.3) All Digital Phase Locked Loop for High Speed Clock Generator.

It uses both a digital control mechanism and ring oscillator can be implemented with standard cells. Power dissipation is about 100mW with 3.3 power supply. Phase locked loop is widely used for frequency synthesis application. Jitter is less than ±4% of clock cycle and also it avoid functional failure of the system. Adaptive algorithm can be used to achieve fast lock in time. It yield better testability, programmability, stability and portability over difficult process and reduces turnaround time. Loop filter detects the maximum and minimum control code. Resolution improved about 5 ps by adding fine tuning delay cell. It has fine tuning range. Controllable range of fine tuning delay cell should cover coarse tuning. Control code has small variation due to input jitter. Fast locking achieves 41 refresh cycles has better portability. It is suitable for on chip application. Pulse amplifier effectively minimize dead zone of the signal.

2.4) A Anti Reset all Digital Delay Locked Loop.

Input clock frequency changes significantly, the dynamic frequency detector relocks digital locked loop without any external reset signal. Binary time to digital converter used to reduce the hardware requirement. It takes six cycles to synchronize input and output signals. It used to de skew buffer and clock generator and also achieves low cost, wide operating frequency, low jitter and low power consumption. It has short lock time, easy migration with poor jitter performance. Process sensitive characteristics make them difficult to migrate in advanced technology. The residual phase error can be corrected by phase detector and counter. However it increases lock time. Power consumption is about 10mW. Peak to peak jitter is about 11.78ps. Internal reset is active to relock pulse. Delay is closed to half period of input clock, residual phase error between input and output is small.

## 3. PROPOSED SOLUTION

In existing method glitch is removed by using NAND gate and delay is reduced in digital manner. Power consumption is more. In proposed system universal gate is used for low power consumption of circuit.

3.1) Removal of Glitch in circuit

Glitching problem will occur when the control code of circuit struck at some values and it gives error values at the output. Glitching problem can be solved by raising the control values of the cells in each element of the circuit.

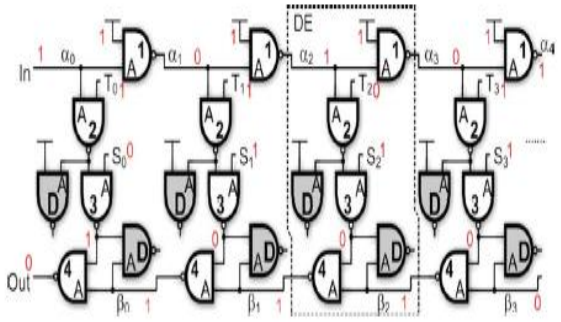


Fig.1 Inverting Glitch Free Circuit of NAND Gate

The circuit eliminates the presence of glitches by using dummy cells in each element of circuit. Control bits can in one of the three possible states. In pass state the circuit with universal gate of third element gives output 1 and fourth element makes the signal propagate to low level of gates in the circuit. In this figure all the NAND gates present same load and gives same delay. Delay is given by

$$\delta = 2t_{nand} + 2t_{nand}.c$$

Where $t_{nand} = (t_{nand\ LH} + t_{nand\ HL})/2$

While tnand LH and tnand HL represent the delay of each NAND gate for low to high and high to low output commutation respectively.

When delay cell is passed to output of third element of gate it becomes post turn state and all other state become turn state. Signal propagates from input to output of the circuit through gates. Dummy cells are used to maintain load balancing in the circuit. The NAND gate is used to reduce the hardware of circuit. Any gate can be constructed with help of NAND gate. It is very useful for construction of digital circuits.



 

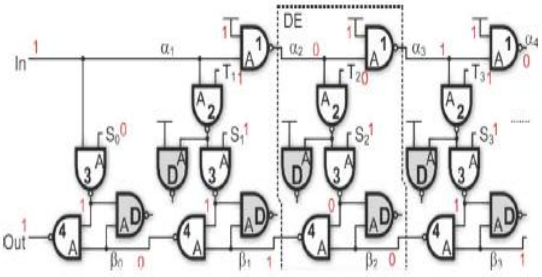


Fig.2 Non Inverting Glitch Free Circuit of NAND Gate.

In many applications output glitching can be avoided by synchronizing both input and output values. Minimizing the arrival time of control bit values than input values to reduce the delay time of each element.

3.2) Power Analyses for Circuit using NAND gate.

Table 1: Power analyses for NAND gate Circuit.

| Power analysis | Power consumption of circuit using NAND gate (μW) [existing method] | Power consumption of circuit using NAND gate. (μW) [Proposed method] |
|---|---|---|
| Glitching circuit | 0.92μW | 0.036 μW |
| Inverting circuit | 1.33 μW | 0.047 μW |
| Noninverting circuit | 1.33 μW | 0.042 μW |

Power consumption for the circuit constructed using NAND gate is reduced than existing method with help of 45nm technology. Performance of circuit is also maintained same by removing the glitches and results obtained for both circuit. In 45nm technology leakage current is reduced. It has higher density and higher switching performance. Power consumption of NAND gate is than the power consumption of circuit with combination of AND and INVERTER gates.

3.3) Implementation of circuit using NOR gate

Circuit is also implemented using NOR gate to reduce the power consumption of the circuit. Power consumption of NOR gate is less than the power consumption of NAND gate and it increases the speed of operation of given circuit. Implementation of circuit using universal gate reduce hardware its requirement.

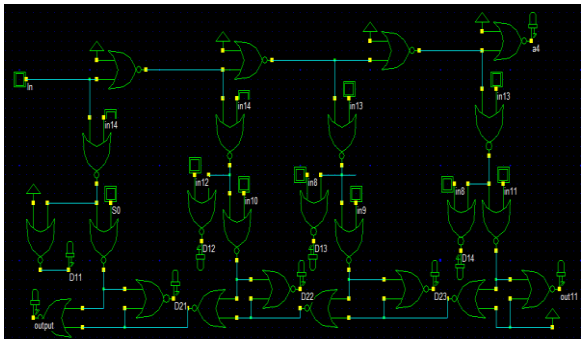

Fig.3 Inverting Circuit using NOR gate.

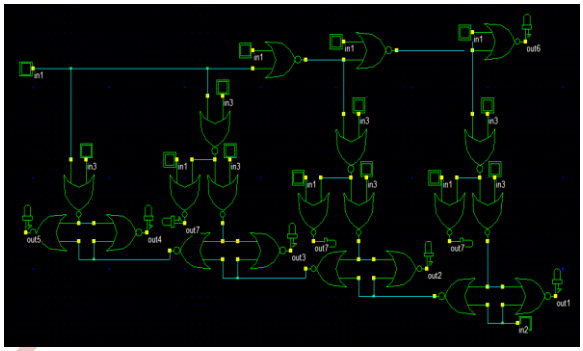

Fig.4 Non inverting circuit using NOR gate.

3.4) Power Analyses for circuit using NOR gate.

Table 2: Power Analyses for NOR gate Circuit.

| Power analysis | circuit using NAND gate (32nm) | Circuit of NOR gate (32nm) |
|---|---|---|
| Glitching circuit | 0.118 μW | 4nW |
| Glitch free inverting circuit | 0.152 μW | 7nW |
| Glitch free non inverting circuit | 0.149 μW | 6nW |

Power consumption of circuit using NOR gate is less in 32nm technology. It reduces fabrication cost. It increases operating speed and dissipates less power than 45nm technology.

## 4. CONCLUSION

The universal gate based digitally controlled delay cells are used to reduce delay to produce output and also it removes the glitches present in the circuit. Power consumption of NAND gate is reduced than existing method. Circuit implemented using NOR gate also reduces power consumption. It also has better performance.



 

## 5. ACKNOWLEDGEMENT

We would express sincere thanks to our supervisor for his valuable comments and active support to our work.

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