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MSIC Vector Used in BIST for Power Reduction by Selective Trigger scan Architecture

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***Abstract*— BIST techniques can effectively reduce the difficulty and complexity of VLSI testing by introducing on-chip test hardware into the circuit-under-test. A method of test pattern generator (TPG) for built-in self-test, based on generation of multiple single input change (MSIC) vectors in a pattern with selective trigger scan architecture, i.e., each vector applied to a scan chain is an SIC vector. This method generates test pattern without additional hardware. This architecture reduces switching activity in the circuit-under-test (CUT) and increases the clock frequency of the scanning process. An auxiliary chain is utilized in this architecture to avoid the large number of transitions to the CUT during the scan-in process, as well as enabling retention of the currently applied test vectors and applying only necessary changes to them. The auxiliary chain shifts in the difference between consecutive test vectors and only the required transitions (referred to as trigger data) are applied to the CUT. Power requirements are substantially reduced. Data reformatting is applied in order to make the proposed architecture amenable to data compression, thus permitting a further reduction in test time. It also permits delay fault testing. Using ISCAS 85 and 89 benchmark circuits, the effectiveness of this architecture for improving SoC test measures (such as power, time, and data volume) is experimentally evaluated and confirmed.**

***General terms* — Built-in self-test (BIST), single-input change (SIC), test pattern generator (TPG), Scan test, test data volume, test application time, test power, test compression, delay testing.**

I. INTRODUCTION

As the number of cores on a chip is increasing the amount of total test data required for testing such systems is growing rapidly. This may pose serious problems because of the cost and technological limitations (like speed and memory capacity) of the automated test equipment (ATE). One of the well-known solutions to this problem is to use BIST and to perform test pattern generation and output response compaction on the chip by using pseudorandom patterns. Due to several reasons like very long test sequences and random pattern resistant faults this approach may not always be efficient. Therefore Multiple Single Input Change Vector (MSIC) approaches have been proposed where pseudorandom test patterns are complemented with deterministic test patterns which are applied from the ATE or in special situations, from the on chip memory. MSIC compared to the pure deterministic testing while providing higher fault coverage and reduced test times and power compared to the stand-alone BIST solution. Test time and test data volume. Application time is one of the sources of complexity when testing IP cores as commonly found in SoCs. Random or deterministic vectors are either generated by on-chip hardware for built-in self-test (BIST) or provided by an external tester such as automatic test equipment (ATE) for manufacturing test. For testing logic blocks, the feasibility of on-chip test generation is mainly restricted to (pseudo)random methods. In general, the area overhead required by a dedicated (on-chip deterministic) vector generation is rather prohibitive for manufacturing test.

A. Related Previous Work

Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard *et al.* analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction. The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Corno *et al.* provided a low-power TPG based on the cellular automata to reduce the test power in combinational circuits [6]. Another approach focuses on modifying LFSRs. The scheme in reduces the power in the CUT in general and clock tree in particular. In [8], a low-power BIST for data path architecture is proposed, which is circuit dependent.

However, this dependency implies that nondetecting subsequences must be determined for each circuit test sequence. Bonhomme *et al.* [9] used a clock gating technique where two non overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhunia *et al.* [11] inserted blocking logic into the stimulus path of the scan flip-flops

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to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied.

The third class makes use of the prevention of pseudorandom patterns that do not have new fault detecting abilities [15]. These architectures apply the minimum number of test vectors required to attain the target fault coverage and therefore reduce the power. However, these methods have high area overhead, need to be customized for the CUT, and start with a specific seed. Gerstendorfer *et al.* also proposed to filter out non detecting patterns using gate-based blocking logics [16], which, however, add significant delay in the signal propagation path from the scan flip-flop to logic.

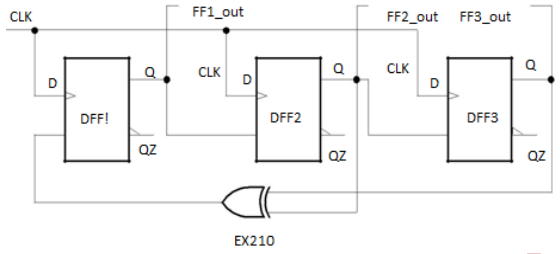

Fig 1. Block Diagram of Linear Feedback Shift Register

Several low-power approaches have also been proposed for scan-based BIST. The architecture in [17] modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scan-enable (SE) inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan-based tests and the peak power in the CUT. In [19], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. Other approaches include LT-LFSR, a low-transition random TPG, and the weighted LFSR. The TPG in can reduce the transitions in the scan inputs by assigning the same value to most neighboring bits in the scan chain. In power reduction is achieved by increasing the correlation between consecutive test patterns. The weighted LFSR in decreases energy consumption and increases fault coverage by adding weights to tune the pseudorandom vectors for various probabilities.

B. Organization of paper and advantage of MSIC

The proposed paper presents the theory and application of a class of minimum transition sequences. This method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. The advantages of the proposed sequence are:

- *Minimum transitions:* In the proposed pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power.
- *Uniqueness of patterns:* The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequence can meet the requirement of the target fault coverage for the CUT.
- *Uniform distribution of patterns:* The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time [23]. It is proved in this paper that our multiple SIC (MSIC) sequence is nearly uniformly distributed.
- *Low hardware overhead consumed by extra TPGs:* The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a sequential decompressor. Hence, the proposed TPG can be easily implemented by hardware.

The rest of this paper is organized in the following Sections are, the proposed MSIC-TPG scheme is presented- The principle of the new MSIC sequences is described - the properties of the MSIC sequences are analyzed- experimental methods and results on test power, fault coverage, and area overhead are provided to demonstrate the performance of the proposed MSIC-TPGs- Conclusions.

II. PROPOSED ARCHITECTURE DESIGN OF MSIC VECTOR

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple code words. Meanwhile, the generated code words will bit XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

A. Method of Generating Test Pattern in MSIC

Assume there are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has l scan cells. Fig 2 shows the symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR

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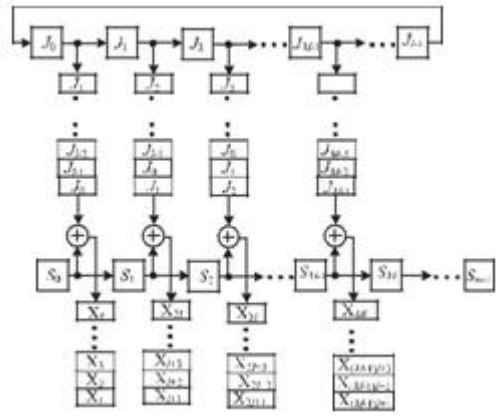
with the primitive polynomial can be expressed as $S(t) = S_0(t)S_1(t)S_2(t), \ldots, S_{m-1}(t)$ (hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as $J(t) = J_0(t)\ J_1(t)\ J_2(t), \ldots, J_{l-1}(t)$.

In the first clock cycle, $J=J_0J_1J_2\ldots J_{l-1}$ will bit-XOR with $S=S_0S_1S_2\ldots S_{M-1}$,and the results $X_1X_{l+2}X_{2l+2},\ldots X_{(M-1)l+1}$ will be shifted into M scan chain. In second clock cycle, $J=J_0J_1J_2\ldots J_{l-1}$ will be circularly shifted as $J= J_{l-1}\ J_0J_1J_2\ldots J_{l-2}$ it will also bit-XOR with the seed $S=S_0S_1S_2\ldots S_{M-1}$.The resulting $X_2X_{l+2}X_{2l+2},\ldots X_{(M-1)l+2}$ will be shifted into M scan chain .

After $l$clock, each scan chain will be fully loaded with a unique Johnson codeword, Since the circular Johnson counter can generate l unique Johnson codewords through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig.2 actually constitute a linear sequential decompressor.



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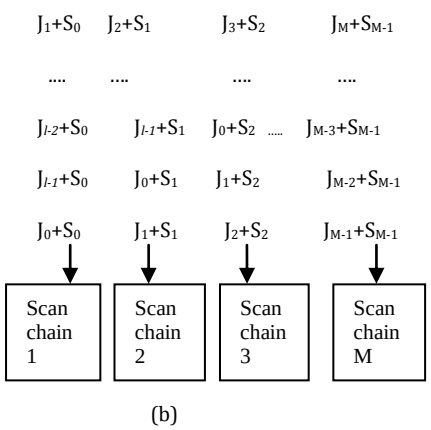


(b)

Fig 2. (a) Simulation of MSIC Pattern for Scan Chain.
(b)Symbolic representation of an MSIC pattern.

B.Generation of test pattern in Johnson Counter

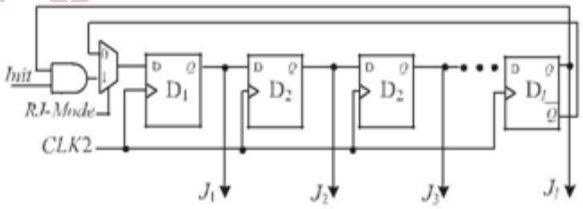
According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson codeword, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

Operation of Johnson counters:

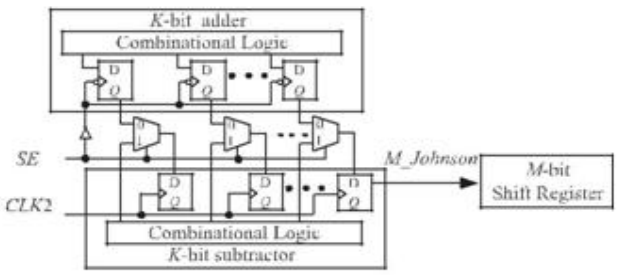
For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig. 3(a), it can operate in three modes.

Initialization: When RJ_Mode is set to 1 and *Init* is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.

- *Circular shift register mode:* When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.
- *Normal mode:* When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate $2l$ unique SIC vectors by clocking CLK2 $2l$ times.



(a)



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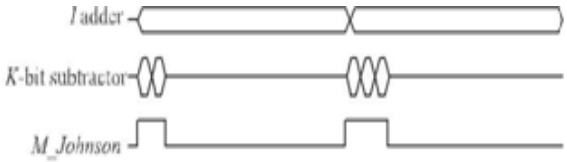


(c)

Fig. 3 SIC generators. (a) Reconfigurable Johnson counter. (b) Scalable SIC counter.(c)Waveforms of the scalable SIC counter.

C.Scalable SIC Counter for large scan length

When the maximal scan chain length l is much larger than the scan chain number M, we develop an SIC counter named the "scalable SIC counter." As shown in Fig.3 (b), it contains a k-bit adder clocked by the rising SE signal, a k-bit subtractor clocked by test clock CLK2, an M-bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of $\log_2 (l - M)$. The waveforms of the scalable SIC counter are shown in Fig. 3(c). The k-bit adder is clocked by the falling SE signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 3(b), it can operate in three modes.

1) If SE = 0, the count from the adder is stored to the k-bit subtractor. During SE = 1, the contents of the k-bit subtractor will be decreased from the stored count to all zeros gradually.
2) If SE = 1 and the contents of the k-bit subtractor are not all zeros, M-Johnson will be kept at logic 1 (0). Otherwise, it will be kept at logic 0 (1). Thus, the needed 1s (0s) will be shifted into the M-bit shift register by clocking CLK2 l times, and unique Johnson codeword will be applied into different scan chains.

For example, after full-scan design, ISCAS'89 s13207 has 10 scan chains whose maximum scan length is 64. To implement a scalable SIC counter as shown in Fig. 3(b), it only needs 6 D-type flip-flops (DFFs) for the adder, 6 DFFs for the subtractor, 10 DFFs for a 10-bit shift register for 10 scan chains, 6 multiplexers, and additional 19 combinational logic gates. The equivalent gates are 204 in total. For a 64-bit Johnson counter, it needs 64 DFFs, which are about 428 equivalent gates. The overhead of a MSIC-TPG can thus be effectively decreased by using the scalable SIC counter.

Generally, the gate overhead of a MSIC-TPG can be estimated by the number of DFFs (N_{DFF}) used

$$N_{DFF} = m + M + 2log_2 l = (m + M)(1 + \frac{2log_2 l}{m + M})$$

where m, M, and l are the seed number, scan chain number, and the maximum scan length, respectively. The number of DFFs does not vary with the CUTs' sizes. For example, as will be shown in Table II, for ISCAS'89 benchmarks, when the seed number increases from 20 to 38 and the maximum scan length increases from 54 to 87, their area overheads change only from 397.40 to 488.29 μm^2.

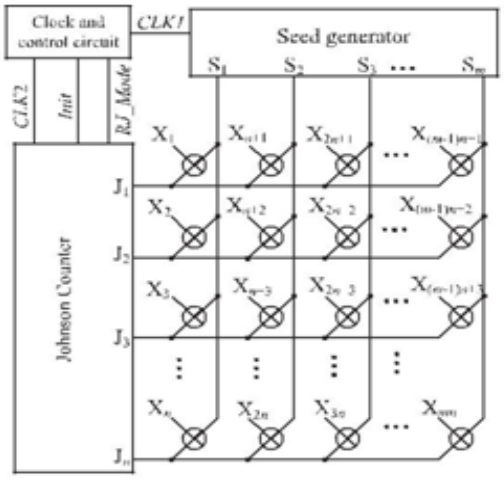
D. Test-Per-Clock in MSIC-TPG

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 4(a). The CUT's PIs $X_1 - X_{mn}$ are arranged as an $n \times m$ SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m-stage conventional LFSR, and operates at low frequency CLK1. The test procedure is as follows.

1) The seed generator generates a new seed by clocking CLK1 one time.
2) The Johnson counter generates a new vector by clocking CLK2 one time.
3) Repeat 2 until 2l Johnson vectors are generated.
4) Repeat 1–3 until the expected fault coverage or test length is achieved.

E. Test-Per-Scan in MSIC-TPG

The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 4(b). The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to M scan chains, respectively. The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.



(a)

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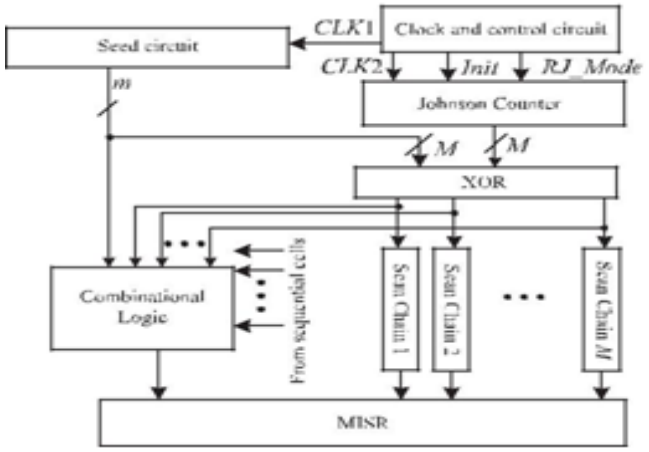


(b)

Fig. 4. MSIC-TPGs for (a) test-per-clock and (b) test-per-scan schemes.

1) The seed circuit generates a new seed by clocking CLK1 one time.
2) RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3) After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates *l* codewords by clocking CLK2 *l* times. Then, a capture operation is inserted.
4) Repeat 2–3 until 2*l* Johnson vectors are generated.
5) Repeat 1–4 until the expected fault coverage or test length is achieved.

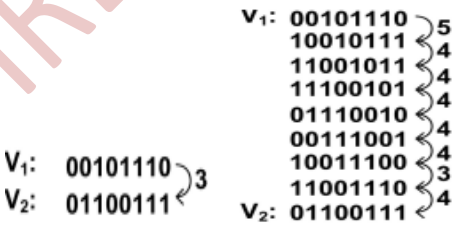
III. DESIGN OF SELECTIVE TRIGGER SCAN ARCHITECTURE

This work proposes a novel scan architecture that is referred to as the Selective Trigger Scan Architecture (STSA). This scan architecture uses a triggering (enabling) chain in addition to the data registers. Furthermore, triggering chain hardware is designed to take advantage of similar adjacent data for test compression.

A. Architectural Functionality

In selective trigger scan architecture, instead of shifting new serial data into the data registers, the triggering chain decides where a data flip-flop must toggle or retain its old value. Retaining data causes a small number of transitions at the data register outputs and low power dissipation. Along with test reformatting techniques, this architecture can reduce test time and power. It can also reduce data volume by enabling the application of compression algorithms on its reformatted data. This structure can be used as a core or chip-level design-for-test (DFT) technique. In addition, it is applicable to delay fault testing. When applied at the core level, substantial improvements in power and test time can be achieved by reformatting the precomputed vectors rather than starting with a new set of tests.

Our proposed architecture with a simple example. Let us assume that V_1 in Fig.5a is an existing test vector in a scan chain and V_2 is the next test vector that must be shifted. Comparing V_1 and V_2 transitions (Fig. 5a), there are only three differences in their bits that are called necessary transitions. If we were to use a standard scan chain and shift V_2 into the scan chain in eight test clocks, with each shift, transitions shown in Fig. 5b would occur. For example, shifting the rightmost 1 of V_2 into the scan chain causes five transitions in the eight scan flip-flops. All together, shifting V_2 would cause 32 transitions that are called unnecessary transitions. On the other hand, parallel loading V_2 directly into our architecture eliminates un-necessary transitions on the input of a CUT.



(a) (b)

Fig 5. (a) Necessary transitions between two consecutive test vectors(three transitions).
(b) Total number of unnecessary transitions in conventional scan architecture (32 transitions).

Hence, our scan architecture should eliminate the unnecessary transitions. In addition, the following features should be considered for the proposed scan architecture and DFT method:

- A scan architecture should not add extra inputs compared to a conventional scan approach.
- A DFT approach must add no delay to the normal operation of the circuit.

B. Selective Trigger Scan Chain for Power Reduction in MSIC Pattern

In this architecture, shown in Fig. 6, serves two purposes. One is to reduce the activity at the data outputs

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and the second is to facilitate test data compression. As shown in Fig. 6, this architecture has data registers that contain the test data applied to the CUT, a triggering chain where the test data is shifted in, and a triggering logic circuit with an enabling AND that determines how the test data should be decoded and trigger the data registers.

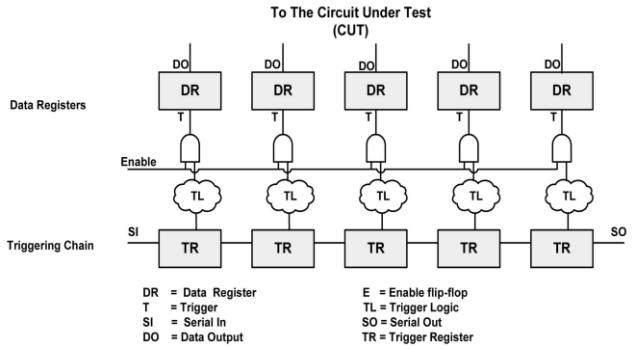

Fig 6. Architecture of Selective Trigger Scan-Chain.

The triggering chain is for reducing the activity at the data register outputs. For this purpose, instead of shifting test vectors into the data registers, triggering data is obtained by formatting test vectors and shifted into the triggering chain.

C.Triggering Logic

The triggering logic is implemented by an XOR gate. Fig. 7 shows the structure of a scan cell of the proposed scan chain. In this case, for the two aforementioned test vectors, 01101101 should be shifted into the triggering chain. This is formed by the XOR of adjacent bits of the difference vector 01001001, starting from the right-hand side.

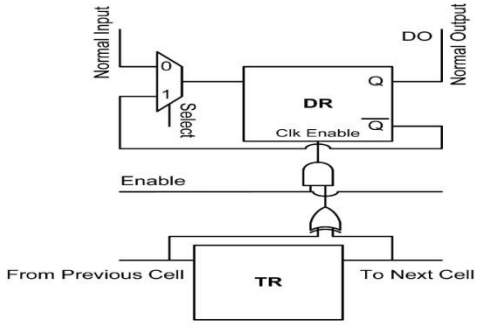

Fig 7.Scan Cell Structure for Selective Trigger Architecture

As shown in Fig. 7, the DR flip-flops is the main storage cell and contains the vector that must be applied to the CUT. The TR chain provides the data required for selective triggering. Testing starts by resetting the DR chain. The TR chain cell has three modes of operation: Shift, Trigger, and Normal. The Shift and Trigger modes are used for testing, while the Normal mode is used for normal operation of the circuit. Table 1 shows the cell configuration in the different operational modes.

TABLE 1
Different Operation Modes in Scan Cell Structure

Operation Modes	Enable	Select	T Chain
Shift	0	1	-
Trigger	1	1	Triggering data
Normal	1	1	101010...

- In the Shift mode, the Enable signal is low (inactive) and the DR flip-flops remain unchanged. Therefore, the required data can be shifted in the TR chain with no effect on the contents of the DR flip-flops.
- In the Trigger mode, the Enable signal is high (active) and the multiplexer selects the input connected to the Q output of DR flip-flops. If the XOR output is 0, the DR flip-flop value will not change. If the XOR output is 1, the value of the DR flip-flop is inverted. Therefore, in the Trigger mode, a 1 at the XOR output of a cell causes an inversion of the value stored in its DR flip-flop. This is accomplished by storing different values in the TR flip-flops of this cell and its neighboring cell (to the left).
- In the normal mode, the TR chain is loaded with a sequence of alternating 1s and 0s (1010 . . .). This activates the outputs of all XORs; by selecting the normal input of the multiplexer and setting the Enable signal to the desired value, each cell performs its normal operation. The loading process of the TR chain with 1010. . . is performed only once, that is, when the test process is completed and the circuit starts its normal operation. During the test, each new vector is obtained through a vector update cycle.

IV. POWER REDUCTION IN TEST MODES

One of the main features of the proposed architecture is to prevent unnecessary transitions from affecting the CUT by altering a conventional scan chain. As the required transitions are only a small portion of the total transitions made during scanning, a reduction in transitions will affect power consumption. This is accomplished using the so-called trigger data; in the proposed architecture, trigger data is transferred from the TR chain because its transitions have a less significant effect on power

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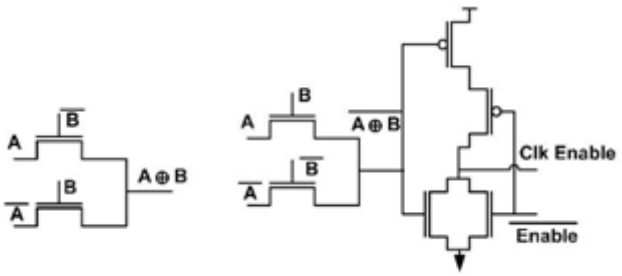
dissipation. A transition in the TR chain will affect only one XOR gate. Cells in the TR chain change only in the Shift mode i.e. the Enable signal is 0. Therefore, transitions in the TR chain can only affect the XOR gate and are masked by the 0 input of the AND gate.

The so-called TR transitions have substantially less impact than the transitions in the DR Chain. This architecture also reduces the number of TR chain transitions by using XORs. The use of XORs makes it possible to send the same difference information with a smaller number of transitions in the TR flip-flops. Without the XOR gates, enabling a DR flip-flop at a specific position would require shifting a 1 to that position in the TR chain, thus resulting in two transitions (a high-to-low and a low-to-high transition) per shift passing through the TR chain. When using XORs, only the difference between two adjacent TR flip-flops at a given position is required, that is, only one transition must pass through the TR chain to reach the specified position. Although it may seem that adding XORs could result in a significant area overhead, these gates can be efficiently implemented in terms of area. As most flip-flops provide both the Q and its complement Q^0, XOR functionality can be provided by using only two transistors in a pass-transistor-based structure, as shown in Fig. 8a. This implementation of the XOR not only has a small impact on area, but its effects on power consumption are negligible due to its pass-transistor-based structure. As shown in Fig. 8b, the logic required for providing the Clk Enable signal to each DR flip-flop requires only six transistors to implement the functionality of both the XOR and AND gates in Fig. 8.



(a) (b)

Fig 8. (a) A two-transistor XOR. (b) The structure used for implementing the Clk Enable signal of the DR flip-flops.

A.Strollo et al. [23] have introduced new designs for gating the clock in D-type flip-flops to reduce power consumption. These D-type flip-flops are best suited for applications in which the data switching activity is low, such as with the TR chain. These D-type flip-flops use a comparator to determine whether the new data is identical to the previous state of the flip-flop. If not, the comparator output activates the clock and the new data is clocked in. Else, the clock of the D-type flip-flop is disabled by the comparator.

The comparator is an XOR gate in which its inputs are connected to the flip-flop inputs and output lines. As mentioned previously, the switching activity in the TR chain is low, so this D-type flip-flop can be used to reduce the power consumption when scanning the data in the TR chain. As XOR gate compares the input of the TR cell with its output. With the D-type flip-flop in the TR cells, the XOR gate can be removed by using the output of the built-in XOR of the D-type flip-flop. The inverter used for inverting the D input is not required because the D input of each cell is the Q output of the previous cell (whose inverted value is also available).

So by using this selective trigger scan architecture in MSIC pattern for scan chain we future reduce power compare to LFSR and without selective trigger in MSIC scan chain. To analyze the performance of the proposed MSIC-TPG, experiments on ISCAS'85 benchmarks and standard full-scan designs of ISCAS'89 benchmarks are conducted. The performance simulations are carried out with the Synopsys Design Analyzer and Prime Power. The test frequency is 100 MHz, and the power supply voltage is 1.1 V. The test application method is test-per-clock for ISCAS'85 benchmarks and test-per-scan for ISCAS'89 benchmarks.

For ISCAS'85 benchmarks, the area overheads of MSIC and LFSR are 21%–157% and 22%–258%, respectively. The MSIC-TPG thus incurs less area overhead than the LFSR. Taking c2670's TPGs for example, the LFSR TPG contains 233 DFFs and 3 XOR gates, while the MSIC-TPG contains 233 XOR gates in the XOR array, 16 DFFs in the Johnson counter, 15 DFFs and 3 XOR gate in the seed generator, and 67 additional logic gates for the control and clock circuit. The number of total equivalent gates is about 2309 for the conventional LFSR and 1089 for the MSIC-TPG. So area is also reduce in MSIC-TPG.

V. SIMULATION RESULT

MODEL SIM simulation of Johnson counter and scalable SIC counter are simulated and test pattern are generated.

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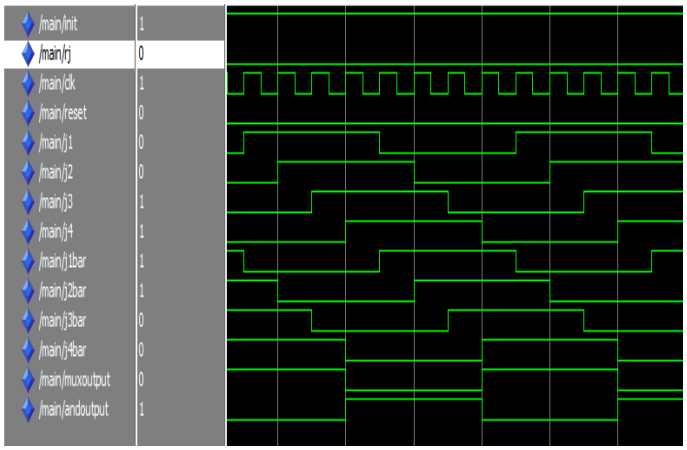
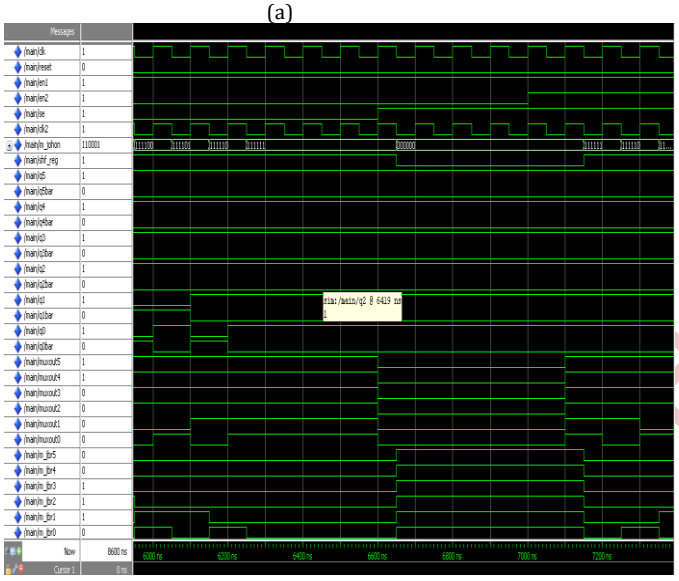


(a)



(b)

Fig 9.(a)Waveform of Johnson counter.(b)Waveform of Scalable SIC counter.

VI. CONCLUSION

In low-power test pattern generation method that could be easily implemented by hardware. Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and is flexible to test-per-clock schemes and test-per-scan schemes. This paper has proposed a scan architecture that considerably improves SoC testing in terms of power and time. Power consumption is reduced during the test process by preventing transitions in the scan chain from spreading into the CUT. Data in this architecture is scanned at higher clock frequencies because no MUX is introduced in the critical scanning path .It was shown that the proposed architecture can also be used for reconstructing the original test vectors from their differences within a compressed data stream. The applicability of the proposed architecture to compression leads to a shorter test time and reduces ATE memory requirements. Analysis results demonstrate that the MSIC-TPG using selective trigger scan architecture is scalable to scan length it also reduce power in test mode.

REFERENCES

[1] P. Girard, "Survey of low-power testing of VLSI circuits," *IEEE Design Test Comput.*, vol. 19, no. 3, pp. 80–90, May–Jun. 2002.

[2] A. Abu-Issa and S. Quigley, "Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 5, pp. 755–759, May 2009.

[3] S. Wang and S. Gupta, "DS-LFSR: A BIST TPG for low switching activity," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 7, pp. 842–851, Jul. 2002.

[4] F. Corno,M. Rebaudengo, M.Reorda,G.Squillero, and M.Violante,"Low power BIST via non linear hybrid cellular automata,"in proc.18th IEEE VLSI Test symp., Apr-May 2000, pp 29-34.

[5] D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian, "Low power/energy BIST scheme for datapaths," in *Proc. 18th IEEE VLSI Test Symp.*, Apr.–May 2000, pp. 23–28.

[6] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravos-soudovitch, "A gated clock scheme for low power scan testing of logic ICs or embedded cores," in *Proc. 10th Asian Test Symp.*, Nov. 2001, pp. 253–258.

[7] C. Laoudias and D. Nikolos, "A new test pattern generator for high defect coverage in a BIST environment," in *Proc. 14th ACM Great Lakes Symp. VLSI*, Apr. 2004, pp. 417–420.

[8] S.Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-power scan design using first-level supply gating," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 3, pp. 384–395, Mar. 2005.

[9] X. Kavousianos, D. Bakalis, and D. Nikolos, "Efficient partial scan cell gating for low-power scan-based testing," *ACM Trans. Design Autom. Electron. Syst.*, vol. 14, no. 2, pp. 28-1–28-15, Mar. 2009.

[10] F. Corno, M. Rebaudengo, M. Reorda, and M. Violante, "A new BIST architecture for low power circuits," in *Proc. Eur. Test Workshop*, May 1999, pp. 160–164.

[11] S.Gerstendorfer and H.-J. Wunderlich, "Minimized power consumption for scan-based BIST," in *Proc. Int. Test Conf.*, Sep. 1999, pp. 77–84.

[12] A. Hertwing and H. Wunderlich, "Low power serial built-in self-test," in *Proc. Eur. Test Workshop*, 1998, pp. 49–53.

[13] S. Wang and W. Wei, "A technique to reduce peak current and average power dissipation in scan designs by limited capture," in *Proc. Asia South Pacific Design Autom. Conf.*, Jan. 2007, pp. 810–816.

[14] N. Basturkmen, S. Reddy, and I. Pomeranz, "A low power pseudo-random BIST technique," in *Proc. IEEE Int. Conf. Comput. Design: VLSI Comput. Process.*, Sep. 2002, pp. 468–473.

[15] S. F. Q. Abdallatif and S. Abu-Issa, "Multi-degree smoother for low power consumption in single and multiple scan-chains BIST," in *Proc. 11th Int. Symp. Qual. Electron. Design*, Apr. 2010, pp. 689–696.

[16] Y. Zorian, "A Distributed BIST Control Scheme for Complex VLSI Devices," Proc. IEEE VLSI Test Symp., pp. 4-9, 1993.

[17] S. Wang and S.K. Gupta, "ATPG for Heat Dissipation Minimiza-tion

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during Scan Testing," Proc. IEEE Design Automation Conf., 614-619, 1997.

[18] A. Wang and S. Gupta, "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," Proc. IEEE Int'l Test Conf., pp. 85-94, 1999.

[19] A. Strollo, E. Napoli, and D. De Caro, "New Clock-Gating Techniques for Low-Power Flip-Flops," Proc. Int'l Symp. Low Power Electronics and Design, pp. 114-119, July 2000.

[20] S. Sharifi, J. Jaffari, M. Hosseinabady, Z. Navabi, and A. Afzali-Kusha, "A Scan-Based Structure with Reduced Static and Dynamic Power Consumption," J. Low Power Electronics, vol. 2, no. 3, pp. 477-487, Dec. 2006.

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