

# Implementation and Optimization of 16×16 Luminance and 8×8 Chrominance Intra Prediction on FPGA

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**Abstract:** This paper proposes an efficient design and implementation of 16×16 block size luminance [2,3] and 8×8 block size chrominance[2] intra prediction. In H.264 intra prediction is used to remove spatial redundancy in a frame because there is correlation between neighbouring pixels in a frame. In this project luminance(Y) and chrominance (Cb,Cr) are intra predicted by dividing Y frame to a size of 16×16 and Cb,Cr frame to a size of 8×8. Video is processed in YCbCr format because human eye is more sensitive to luminance than chrominance part. Four modes of luminance Y and four modes each for chrominance Cb, Cr is optimized and implemented on FPGA. Parallel design is carried out to process all modes to achieve less latency. The design is created in Verilog using Xilinx ISE and simulated using ISIM. This design is synthesized and implemented on Virtex-6 (Device: xc6vcx130T, Package: ff484, Speed:-2) FPGA. The results got are analyzed and power consumption is estimated using Xilinx Xpower Analyzer. This research can be used in various video compression hardware applications.

**Keywords:** H.264, Luminance, Chrominance, Intra Prediction, synthesize, FPGA.

## I. INTRODUCTION

Video and video related application huge demands have led to various researches in this field. These researches led to innovation of H.264 [1] advanced video coding(AVC). The basic coding structure of H.264 is show in Fig.1. H.264 is method which is used to encode the video so that it can be stored using less memory. H.264 uses various algorithm and process to compress an raw video. Intra prediction is one of the process which exploits spatial redundancy in a video frame. As we know there is a high correlation between neighbouring pixels in a frame and these high correlation between pixels in a same frame can be eliminated to achieve compression and video can be reconstructed with small amount of error introduced which is not seen by human eye. The raw video in RGB [2,3,11] (Red, Green, and Blue) format is converted to

luminance and chrominance format (YCbCr)[2,3,11]. Since human eye is more sensitive to luminance part of the image than chrominance part, YCbCr format can be used to efficiently compress a video and reconstructed with good quality. Intra prediction[1,3] for luminance part as two block sizes: 4×4 and 16×16. Chrominance[1,3] part has only one block size 8×8. In intra prediction a luminance frame is divided into 16×16 macroblock and subdivided into 4×4 block. This is called 4×4 luminance intra prediction. If 16×16 blocks is processed at once than its called 16×16 luminance intra prediction. If block size is small image quality is good but processing and memory requirements are high. If block size is big image quality is of average quality but takes less processing time. Depending on application block size can be chosen.

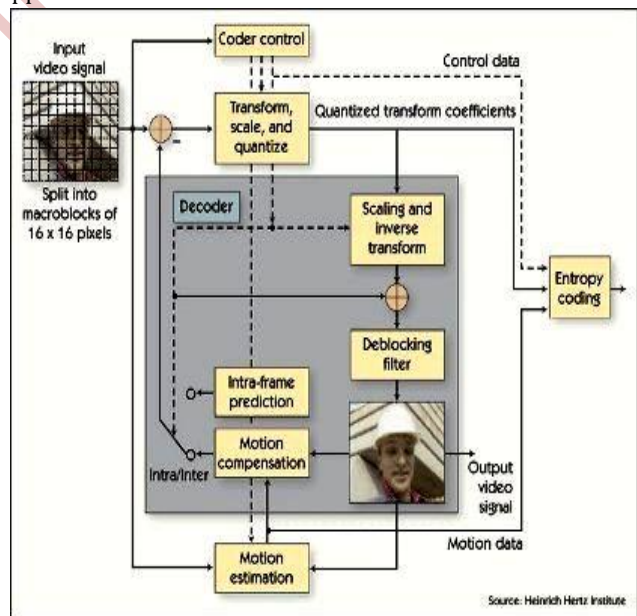


Fig.1. Basic Coding Structure for H.264/AVC.

In this project an efficient parallel approach is designed for 16×16[3] luminance intra prediction and two parts(Cb,Cr) of chrominance intra prediction. Many research project have carried out in this field due to the complex structure of intra prediction.

We have implemented this project on FPGA due to many advantages of present generation FPGA's. New generation FPGA's are faster and has more area to implement complex design and can be compared with ASIC's features. Time to design, test and time to market for FPGA's are less than ASIC. So many researchers and industry now a day's prefer FPGA's rather than ASIC's. The rest of the paper discusses the development and design of efficient approach of 16x16 luminance intra prediction and 8x8 chrominance intra prediction.

The rest of the paper is organized as follows. In Section II, H.264 intra prediction is reviewed. The proposed design is discussed in section III. Section IV discusses about simulation and synthesis results of our design. In the end conclusion and references used are highlighted.

## II. 16x16 Luminance and 8x8 Chrominance Intra Prediction

Intra prediction algorithm [1, 2, 3] is a process to eliminate correlation between neighbouring pixels in a single frame of a video sequence. Neighbouring pixels of reconstructed block in current frame is used for prediction of current block. The 16x16 block size luminance prediction has four modes:

### 1. Mode-0: Vertical

Vertical mode[1,3] for 16x16 block size is same as vertical mode for 4x4 block size, but 16x16 block size vertical mode contains 16 adjacent pixels from the reconstructed block at the top of the current block. The upper samples are extrapolated vertically.

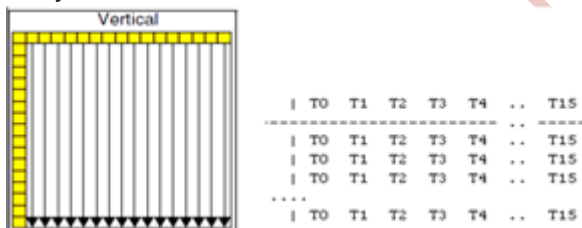


Fig. 2: 16x16 Vertical Prediction.

### 2. Mode-1: Horizontal

Horizontal mode[1,3] for 16x16 block size is same as horizontal mode for 4x4 block size, but 16x16 block size horizontal mode contains 16 adjacent pixels from the reconstructed block at the left side of the current block. The left samples are extrapolated horizontally.

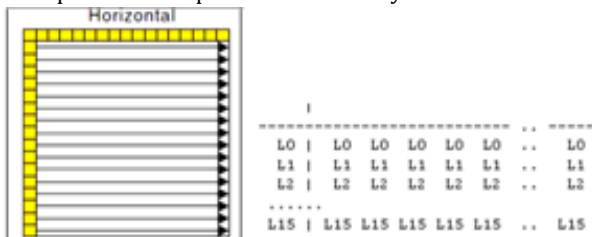


Fig.3: 16x16 Horizontal Prediction.

### 3. Mode-3: DC

Equations for DC[1,2,3] prediction are explained below. If top (T0 to T15) and left (L0 to L15) adjacent reconstructed block neighbour pixels are available then DC prediction is calculated by below formula.

$$\text{Mean} = (\text{sum}(T0 \text{ to } T15) + \text{sum}(L0 \text{ to } L15) + 16) / 32 \quad (1)$$

Else if only top adjacent reconstructed block neighbouring pixels (T0 to T15) are available then DC prediction is calculated by below formula.

$$\text{Mean} = (\text{sum}(T0 \text{ to } T15) + 8) / 16 \quad (2)$$

Else if only left adjacent reconstructed block neighbouring pixels (L0 to L15) are available then DC prediction is calculated by below formula.

$$\text{Mean} = (\text{sum}(L0 \text{ to } L15) + 8) / 16 \quad (3)$$

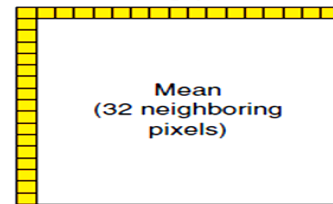


Fig.4: 16x16 DC Prediction.

And if left and top neighbouring pixels are not available then there are no neighbour pixels and mean value 128 is assigned for prediction pixels and is transformed, quantized and encoded.

### 4. Mode-4: Plane Prediction

Plane prediction[1,3] pixels are calculated using following equations.

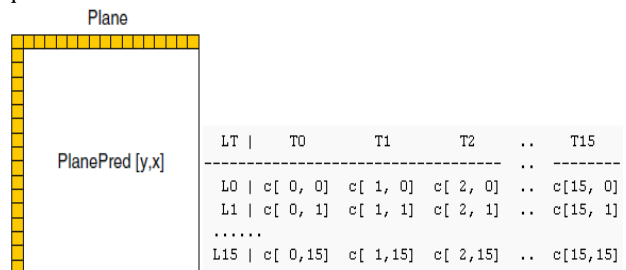


Fig.5: 16x16 Plane Prediction.

$$H = 1 \times (T8 - T6) + 2 \times (T9 - T5) + 3 \times (T10 - T4) + 4 \times (T11 - T3) + 5 \times (T12 - T2) + 6 \times (T13 - T1) + 7 \times (T14 - T0) + 8 \times (T15 - LT). \quad (4)$$

$$V = 1 \times (L8 - L6) + 2 \times (L9 - L5) + 3 \times (L10 - L4) + 4 \times (L11 - L3) + 5 \times (L12 - L2) + 6 \times (L13 - L1) + 7 \times (L14 - L0) + 8 \times (L15 - LT). \quad (5)$$

$$b = (5 \times H + 32) / 64 \quad (6)$$

$$c = (5 \times V + 32) / 64 \quad (7)$$

$$a = (T15 + L15) \times 16 \quad (8)$$

$$\text{Plane Prediction } c(y,x) = \text{saturate\_U8}((a + 16 + b \times (x-7) + c \times (y-7) / 32), x, y = 0 \sim 15). \quad (9)$$

Plane prediction works well in areas of smoothly-varying luminance.

Chrominance part[1,2,3] of the image or frame has two parts Cb and Cr. Both parts are intra predicted separately. Chrominance intra prediction has 4 modes: Mode 0-Vertical, Mode 1-Horizontal, Mode 2-DC and Mode 3-Plane.

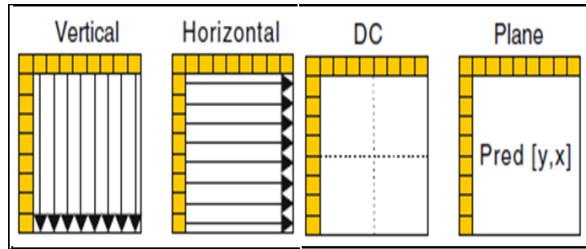


Fig.6: 8x8 Chrominance Modes.

Mode 0, Mode 1 and Mode 2 of 8x8 chrominance intra prediction modes is similar to 16x16 Mode 0, Mode 1 and Mode 2 intra prediction. Only difference is there are 8 pixels in top and left neighbours in 8x8 chrominance mode and 16 pixels in top and left neighbours in 16x16 luminance mode. There is a minor change to the equations of Mode 3 plane prediction which is explained using Fig.7.

LT	T0	T1	T2	T3	T4	T5	T6	T7	T8
L0	Pred[y,x]								
L1									
L2									
L3									
L4									
L5									
L6									
L7									

Fig. 7. 8x8Plane prediction.

$$H = 1 \times (T4-T2) + 2 \times (T5-T1) + 3 \times (T6-T0) + 4 \times (T7-LT) \quad (10)$$

$$V = 1 \times (L4-L2) + 2 \times (L5-L1) + 3 \times (L6-L0) + 4 \times (L7-LT) \quad (11)$$

$$b = (17 \times H + 16) = 32 \quad (12)$$

$$c = (17 \times V + 16) = 32 \quad (13)$$

$$a = (T7 + L7) \times 16 \quad (14)$$

$$\text{Plane Prediction } c(y;x) = \text{saturate } U8(a + 16 + b \times (x-7) + c \times (y-7)) = 32, \quad x,y = 0 \text{ to } 7; \quad (15)$$

### III. DESIGN

This section explains the design of luminance 16x16 intra prediction modes and two chrominance 8x8 modes to implement on FPGA. This project is designed in Verilog using Xilinx ISE tool. The architecture of 16x16 luminance intra prediction is shown in Fig.8. All the modes are processed in parallel[6] to reduce prediction time. Intra predictions control unit controls all the operation. It receives input data, divides video data into blocks and searches neighbours for blocks for intra prediction. It gives control signal to various modes processing unit depending on available neighbours. In section

II depending on neighbours available which modes should be calculated is explained.

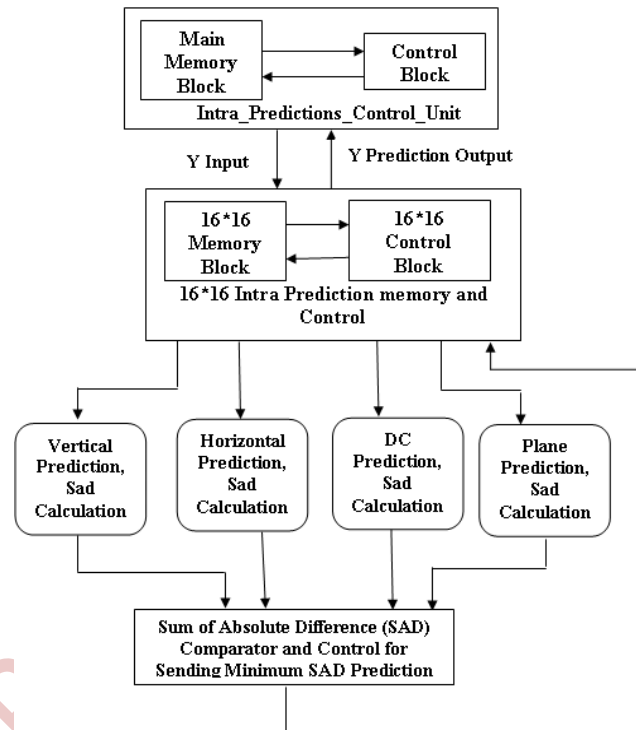
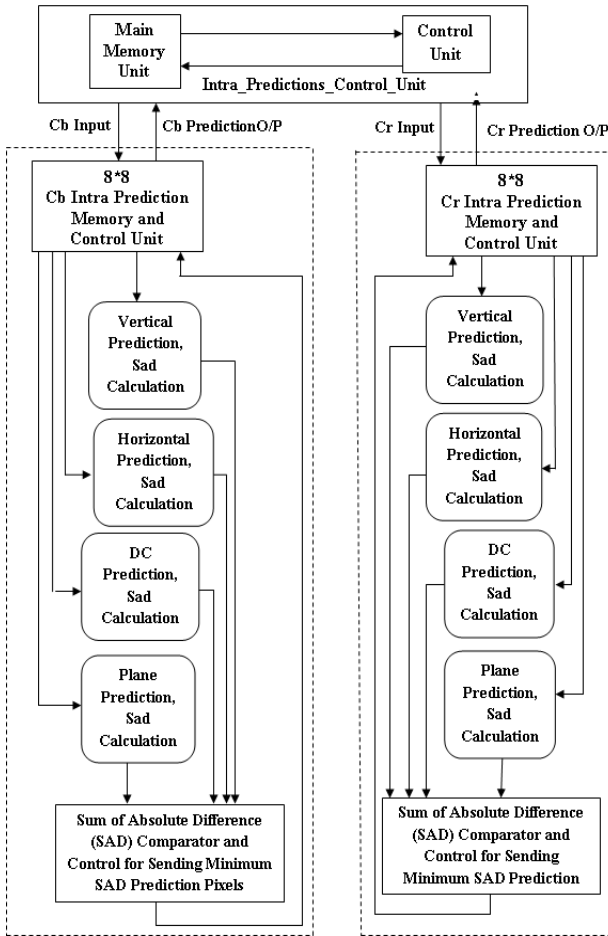


Fig.8: Architecture of Implementation of 4x4 size Luminance Intra Prediction.

Sum of Absolute Differences (SAD) is calculated parallel for every mode by using predicted block pixels and original block pixels. After calculating prediction pixels in all modes the SAD comparator finds the minimum SAD mode and sends the prediction pixels related to that mode to Intra prediction control unit for further processing.

The architecture of chrominance intra prediction is shown in Fig.9. Both Cb and Cr part of chrominance is predicted separately. The four modes for chrominance part are processed in parallel for Cb and Cr part separately as shown in Fig.9. The intra prediction control unit sends original Cb and Cr block pixels and neighbor pixels by dividing frame into block to chrominance Cb and Cr control unit. The chrominance control unit depending on neighbours available sends control signal to start processing modes. SAD is calculated separately for each mode after prediction. After all modes are processed the SAD comparator finds the minimum SAD mode and sends the prediction pixels of that minimum mode to intra predictions control unit for further process. All the calculation in DC mode and plane mode are done using adder, subtractor and multiplication. Multiplication is done using shift and add operations because multipliers uses more FPGA area. Loops are not used in our design for calculation. Instead of loops counters are used.



**Fig.9:** Architecture of Implementation of 8x8 size Chrominance Intra Prediction.

SAD formula is given below:

$$SAD = \sum_{i=0}^N \sum_{j=0}^N C_{i,j} - R_{i,j}$$

Where  $C_{i,j}$  are the original pixels and  $R_{i,j}$  are the prediction pixels for the particular  $16 \times 16$  block in luminance intra prediction. This formula is also same for  $8 \times 8$  chrominance intra prediction. If we implement SAD in conventional way on FPGA it will take more time to calculate SAD. So in this project a new approach is used to implement SAD. As we know original pixels and prediction pixels are in the range of 0 to 255. The 8 bit original and prediction pixel are assigned to two 9 bit registers In SAD equation, we 2's complement 9 bit  $R_{i,j}$  value. And add it with  $C_{i,j}$ . If 9th bit of the result is 1 then 2's complement of result is done to get result. If 9th bit is 0 then there is no 2's complement for the result.

It is explained using example given below.

Consider  $C_{1:1}=198$  and  $R_{1:1}=213$ . Then to calculate sum of absolute difference we assign these two values to 9 bit register  $C1[8:0] = 198 = 011000110$ ;

$R1[8:0] = 213 = 011010101$ ;

Take 2's complement of R1 and add to C1.

$Sum[8:0] = [198-213] = C1 + \sim R1 + 1 = 011000110 + 100101011 = 111110001$ ;

If we consider above result 9th bit is 1. So it implies the result is negative. So we take 2's complement of result. If 9th bit is zero than there is no need of 2's complement to Sum and the Sum result is final answer.

$111110001 = 2's\ complement\ is\ 000001110 + 1 = 1111 = 15$ .

$[|198-213|=15]$ .

SAD is calculated to get error between original block and predicted block. Using SAD value best mode is selected and prediction pixels of that mode are sent to main unit.

#### IV. SIMULATION AND SYNTHESIS RESULTS

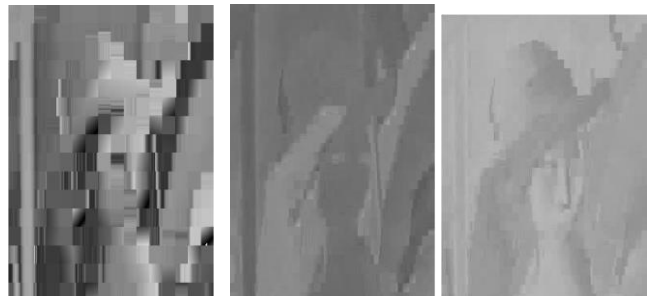
Verilog code for this project is simulated using Xilinx ISIM and verified. The video frame data required for simulation is stored in text file using matlab and given as input by reading text file for simulation using verilog test bench. Simulation result is verified mathematically. Test image used for simulation is shown in Fig.10. The YCbCr component and intra predicted component is shown in Fig.11 and Fig.12.



**Fig.10:** Test Image.



**Fig.11:** Y-Cb-Cr Component.

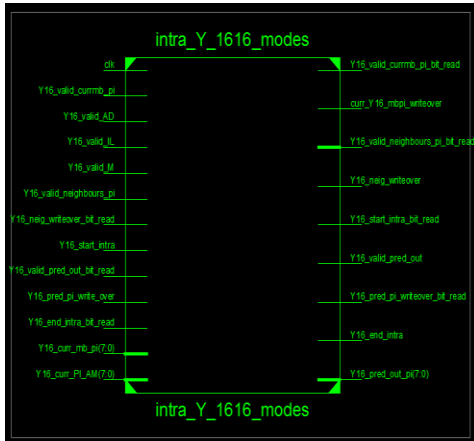


**Fig.12:** 16x16 Y, 8x8Cb, Cr Intra Predicted Component.

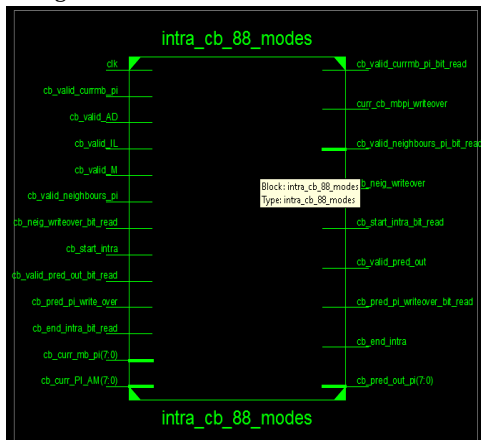
The luminance and chrominance module is synthesized separately using Xilinx XST to find the area occupied by each

module. Designs were implemented on Virtex-6 (Device: xc6vcx130T, Package: ff484, Speed:-2) FPGA.

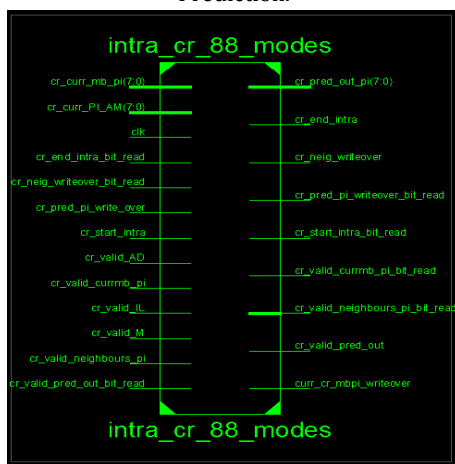
RTL schematic of 16x16 luminance intra prediction is shown In Fig.13.



**Fig.13:** RTL Schematic for 16\*16 Luminance Intra Prediction. RTL schematic of 8x8 chrominance intra prediction is shown in Fig.14 and Fig.15.



**Fig.14:** RTL Schematic for Cb 8\*8 Chrominance Intra Prediction.



**Fig.15:** RTL Schematic for Cr8\*8 Chrominance Intra Prediction.

**Table.1:** Design Summary for 16\*16 Luminance Intra Prediction.

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1,073	1,60,000	1%
Number used as Flip Flops	797		
Number used as AND/OR logics	276		
Number of Slice LUTs	3,546	80,000	4%
Number used as logic	2,890	80,000	3%
Number using O5 and O6	692		
Number used as Memory	624	27,840	2%
Number used as Dual Port RAM	624		
Number of occupied Slices	1,184	20,000	5%
Number of LUT Flip Flop pairs used	3,659		
Number with an unused Flip Flop	2,756	3,659	75%
Number with an unused LUT	113	3,659	3%
Number of fully used LUT-FF pairs	790	3,659	21%
Number of unique control sets	64		
Number of slice register sites lost to control set restrictions	251	1,60,000	1%
Number of bonded IOBs	43	240	17%
Average Fanout of Non-Clock Nets	4.17		

**Table.2:** Design Summary for 8x8 Cb Chrominance Intra.

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	622	1,60,000	1%
Number used as Flip Flops	506		
Number used as AND/OR logics	116		
Number of Slice LUTs	1,888	80,000	2%
Number used as logic	1,723	80,000	2%
Number used as Memory	156	27,840	1%
Number used as Dual Port RAM	156		
Number of occupied Slices	557	20,000	2%
Number of LUT Flip Flop pairs used	1,916		
Number with an unused Flip Flop	1,383	1,916	72%
Number with an unused LUT	28	1,916	1%
Number of fully used LUT-FF pairs	505	1,916	26%
Number of unique control sets	48		

Number of slice register sites lost to control set restrictions	250	1,60,000	1%
Number of bonded IOBs	43	240	17%
Average Fanout of Non-Clock Nets	4.1		
	2		

**Table.3:** Design Summary for 8x8 Cr Chrominance Intra.

Slice Logic Utilization	Used	Available
Number of Slice Registers	626	1,60,000
Number used as Flip Flops	510	
Number used as AND/OR logics	116	
Number of Slice LUTs	1,738	80,000
Number used as logic	1,572	80,000
Number used as Memory	156	27,840
Number used as Dual Port RAM	156	

Number of occupied Slices	536	20,000
Number of LUT Flip Flop pairs used	1,788	
Number with an unused Flip Flop	1,254	1,788
Number with an unused LUT	50	1,788
Number of fully used LUT-FF pairs	484	1,788
Number of unique control sets	48	
Number of slice register sites lost to control set restrictions	254	1,60,000
Number of bonded IOBs	43	240
Average Fanout of Non-Clock Nets	4	

Xilinx XPower Analyzer - intra\_Y\_1616\_modes.ncd - [Table View]

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A	B	C	D	E	F	G	H	I	J	K	L	M	N
<b>Device</b>		<b>On-Chip Power (W)</b>		<b>Used</b>	<b>Available</b>	<b>Utilization (%)</b>	<b>Supply Summary</b>		<b>Total</b>	<b>Dynamic</b>	<b>Quiescent</b>		
Family	Virtex6	Clocks	0.006	1	---	---	Source	Voltage	Current (A)	Current (A)	Current (A)		
Part	xc6vxc130t	Logic	0.012	3546	80000	4	Vccint	1.000	1.094	0.033	1.061		
Package	ft484	Signals	0.015	4437	---	---	Vccaux	2.500	0.075	0.000	0.075		
Temp Grade	Commercial	IOs	0.017	43	240	18	Vcco25	2.500	0.007	0.006	0.001		
Process	Typical	Leakage	1.809				MGTAVcc	1.000	0.303	0.000	0.303		
Speed Grade	-2	Total	1.859				MGTAVtt	1.200	0.213	0.000	0.213		
<b>Environment</b>		<b>Thermal Properties</b>		<b>Effective TJA</b>	<b>Max Ambient</b>	<b>Junction Temp</b>	<b>Supply Power (W)</b>		<b>Total</b>	<b>Dynamic</b>	<b>Quiescent</b>		
Ambient Temp (C)	50.0			(C/W)	(C)	(C)			1.859	0.049	1.809		
Use custom TJA?	No			2.5	80.4	54.6							
Custom TJA (C/W)	NA												
Airflow (LFM)	250												
Heat Sink	Medium Prof												
Custom TSA (C/W)	NA												
Board Selection	Medium (10")												
# of Board Layers	12 to 15												
Custom TJB (C/W)	NA												
Board Temperature (C)	NA												

**Fig.15:** Power Estimation Results for 16\*16 Luminance Intra Prediction.

Xilinx XPower Analyzer - intra\_cb\_88\_modes.ncd - [Table View]

Device		On-Chip	Power (W)	Used	Available	Utilization (%)	Supply Summary		Total	Dynamic	Quiescent
Family	Virtex6	Clocks	0.004	1	---	---	Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc6vxc130t	Logic	0.006	1888	80000	2	Vccint	1.000	1.077	0.017	1.060
Package	ff484	Signals	0.006	2429	---	---	Vccaux	2.500	0.075	0.000	0.075
Temp Grade	Commercial	IOs	0.016	43	240	18	Vcco25	2.500	0.007	0.006	0.001
Process	Typical	Leakage	1.809				MGTAVcc	1.000	0.303	0.000	0.303
Speed Grade	-2	Total	1.841				MGTAVtt	1.200	0.213	0.000	0.213
Environment		Thermal Properties				Effective TJA	Max Ambient	Junction Temp	Supply Power (W)		
Ambient Temp (C)	50.0					(C/W)	(C)	(C)	Total	Dynamic	Quiescent
Use custom TJA?	No					2.5	80.4	54.6	1.841	0.033	1.809
Custom TJA (C/W)	NA										
Airflow (LFM)	250										
Heat Sink	Medium Prof										
Custom TSA (C/W)	NA										
Board Selection	Medium (10")										
# of Board Layers	12 to 15										
Custom TJB (C/W)	NA										
Board Temperature (C)	NA										

Fig.16: Power Estimation Results for Cb 8\*8 Chrominace Intra Prediction.

Xilinx XPower Analyzer - intra\_cr\_88\_modes.ncd - [Table View]

Device		On-Chip	Power (W)	Used	Available	Utilization (%)	Supply Summary		Total	Dynamic	Quiescent
Family	Virtex6	Clocks	0.004	1	---	---	Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc6vxc130t	Logic	0.006	1738	80000	2	Vccint	1.000	1.077	0.017	1.060
Package	ff484	Signals	0.006	2271	---	---	Vccaux	2.500	0.075	0.000	0.075
Temp Grade	Commercial	IOs	0.016	43	240	18	Vcco25	2.500	0.007	0.006	0.001
Process	Typical	Leakage	1.809				MGTAVcc	1.000	0.303	0.000	0.303
Speed Grade	-2	Total	1.841				MGTAVtt	1.200	0.213	0.000	0.213
Environment		Thermal Properties				Effective TJA	Max Ambient	Junction Temp	Supply Power (W)		
Ambient Temp (C)	50.0					(C/W)	(C)	(C)	Total	Dynamic	Quiescent
Use custom TJA?	No					2.5	80.4	54.6	1.841	0.033	1.809
Custom TJA (C/W)	NA										
Airflow (LFM)	250										
Heat Sink	Medium Prof										
Custom TSA (C/W)	NA										
Board Selection	Medium (10")										
# of Board Layers	12 to 15										
Custom TJB (C/W)	NA										
Board Temperature (C)	NA										

Fig.17: Power Estimation Results for Cr 8\*8 Chrominace Intra Prediction.

The 16x16 luminance and 8x8 chrominance modules were implemented as sub modules in intra predictions control unit shown in Fig.18. This project predicts all luminance (4x4 and 16x16) and chrominance (8x8) intra prediction modes with RGB to YCbCr and YCbCr to RGB conversion module implemented. Design summary of Fig.18 is shown in Table.4.

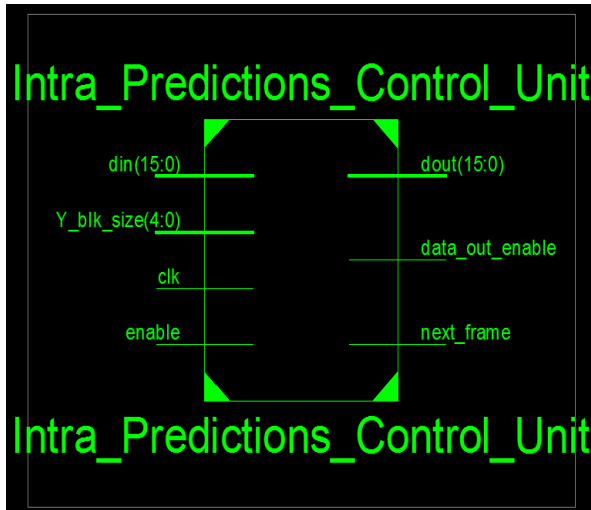


Fig.18: RTL Schematic of Intra Prediction

Table.4: Design Summary of Intra Prediction.

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	5,722	1,60,000	3%
Number used as Flip Flops	4,986		
Number used as AND/OR logics	736		
Number of Slice LUTs	43,554	80,000	54%
Number used as logic	20,641	80,000	25%
Number used as Memory	22,784	27,840	81%
Number used as Dual	22,784		

Depending on user application block size can be decided for luminance intra prediction. Chrominance intra prediction was also implemented effectively with parallel processing for all modes. The results achieved are good compared to previous works. This research can be used in applications related to video coding for faster processing.

### REFERENCES

1. Thomas Wiegand, Gary J. Sullivan, Gisle Bjontega and, and Ajay Luthra, "Overview of the H.264 / AVC Video Coding Standard", *IEEE Trans. On Circuits and Systems for Video Technology*, July 2003.
2. I.Richardson, "The H.264 Advanced video Compression Standard", John Wiley & Sons, 2010.
3. Youn-Long Steve Lin ,Chao-Yang Kao Huang-Chih Ku and Jian-Wen Chen, "VLSI Design for Video Coding- H.264/AVC Encoding from Standard Specification to Chip" *Springer Science+Business Media, LLC* 2010.
4. Muhammad Nadeem, Stephan Wong, and Georgi Kuzmanov, "An efficient hardware design for intra-prediction in H.264/AVC decoder", *Electronics, communications and Photonics Conference (SIEPC)*, 2011 Saudi International.

Port RAM			
Number of occupied Slices	12,315	20,000	61%
Number of LUT Flip Flop pairs used	43,686		
Number with an unused Flip Flop	38,340	43,686	87%
Number with an unused LUT	132	43,686	1%
Number of fully used LUT-FF pairs	5,214	43,686	11%
Number of unique control sets	1,270		
Number of slice register sites lost to control set restrictions	2,842	1,60,000	1%
Number of bonded IOBs	41	240	17%
Number of RAMB36E1/FIFO36E1s	96	264	36%
Average Fanout of Non-Clock Nets	5.88		

### V. CONCLUSION

16x16 luminance intra prediction and 8x8 chrominance intra predictions was effectively designed and implemented on FPGA. FPGA based implementation are very useful for many applications due to less design time and cost. Results shows that 16x16 luminance intra prediction image quality is less than 4x4 luminance intra prediction, the processing time for 16x16 prediction is less than 4x4 prediction.

5. Mikołaj Roszkowski and Grzegorz Pastuszak, "Intra Prediction Hardware Module For High-Profile H.264/AVC Encoder", *Signal Processing Algorithms, Architectures, Arrangements, and Applications Conference Proceedings (SPA)*, 2010.
6. Huailu Ren, Yibo Fan, Xinhua Chen and Xiaoyang Zeng, "A 16-pixel Parallel Architecture with Block-level/Mode-level Co-reordering Approach for Intra Prediction in 4kx2k H.264/AVC Video Encoder", *Design Automation Conference (ASP-DAC)*, 2012 17th Asia and South Pacific.
7. A. Ben Atitallah, H. Loukil and N. Masmoudi, "FPGA Design For H.264/AVC Encoder", *International Journal of Computer Science, Engineering and Applications (IJCSA)*, Vol.1, No.5, October 2011.
8. <http://iphome.hhi.de/suehring/tml/>, "H.264/AVC Software Coordination" JM Reference Software.
9. <http://www.asic-world.com>.
10. [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx14\\_2/xst\\_v6s6.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_2/xst_v6s6.pdf).
11. <http://en.wikipedia.org/wiki/YCbCr>.