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Fully Dynamic Latched CMOS Comparator for Flash Analog to Digital Converters

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Abstract: - *The Dynamic Comparators are the basic building block in an Analog to Digital converters (ADC). The analog signal at the input is amplified into a full scale digital level output signal using cross coupled inverters. This paper describes a CMOS comparator that reduces the overall propagation delay. Comparator design shows that the overall propagation delay of 4.378e-10 seconds and the speed of the clock is 3GHZ with a 1.0 V supply.*

Key-Words: - Comparator, Cmos, Cross Coupled, Delay, Flash ADC's.

1 Introduction

In Today's electronics era Comparators are the basic building blocks in an Analog to Digital Converters. The basic operation in an analog-to-digital Converter (ADC) is to perform comparison between analog signals. The input signal comparisons are carried out by Dynamic latched comparator. Dynamic latched comparator works synchronously with the clock and outputs a digital signal, based on comparison of given input signals. Latched comparators use positive feedback mechanism (aids in the input signal) regenerates (amplifies) the analog input signal into a Full-scale digital level output signal [1]. The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison. The comparator is basically a 1-bit analog-to-digital converter. It is widely used in Analog to Digital converters (ADCs).

The Dynamic latched comparators have an important role in high speed Analog to digital converters. Comparator is the basic circuit that converts analog signal into a digital domain and compares the difference between two inputs and produces binary output signal. The speed, power consumption, delays and offset plays an important role in the designing of the comparators. Instead of using the traditional amplifier-chain type comparators and to obtain a low power dissipation and better speed the dynamic comparators are mostly preferred [2].

Analog to Digital Converters performance majorly depends upon speed and power dissipation. Dynamic latched CMOS comparators are used for many applications such as high-speed analog-to-digital converters (ADCs), data receivers etc due to their fast speed, comparatively reduced power consumption, less delay, high input impedance, and full swing digital level output.

However, an offset voltage, resulting from the transistor mismatches such as threshold voltage *Vth*, current factor *µCoxW/L* and the internal node Capacitances and output load capacitances variations, deteriorates the accuracy of these comparators [3], [4]. Because of the above mentioned points, the input-referred offset voltage is also the important parameters of the design CMOS comparator.

To meet the specifications such as offset voltage and power dissipation in a limited area, it is necessary to fully understand the correlations between sizes of transistors. Conventionally, the latch offset voltage can be reduced by using a pre-amplifier preceding the regenerative latch stage. The major disadvantage or drawback of using a Preamplifier based comparators is that they provide huge static power consumption from the reduced intrinsic gain with a reduction of the drain-to source resistance *rds* due to the continuous technology scaling [9].

2 Recent Developments

Bernhard Wicht et al. (2004) presented "*Latch-Type Voltage Sense Amplifier*" that a quantitative yield analysis of a latch-type voltage sense amplifier with a high-impedance differential input stage and it investigates the impact of supply voltage, input dc level, transistor sizing, and temperature on the input offset voltage.

The input dc level turns out to be most significant. Also, an analytical expression for the sensing delay is derived which shows low sensitivity on the input dc bias voltage. A figure of merit indicates that an input dc level of 0.7V is optimal regarding speed and yield. Experimental results in 130-nm CMOS technology confirm that the yield can be significantly improved by

lowering the input dc voltage to about 70% of the supply voltage. Experimental results show that this dynamic comparator was widely used. However, since this comparator has one tail transistor which limits the total current flowing through the both of the output branches, it shows strong dependency on speed and offset voltage with different common-mode input voltage V_{com}.

Daniel Schinkel et al. (2007) investigated "A Double-Tail Latch-Type Voltage Sense Amplifier" that latch type voltage sense

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amplifier has one tail transistor which limits the total current flowing through the both of the output branches; it shows strong dependency on speed and offset voltage with different common-mode input voltage *Vcom*. To mitigate this drawback, the comparator with separated input-gain stage and output-latch stage was introduced. This separation made this comparator have a lower and more stable offset voltage over wide input common-mode voltage (*Vcom*) ranges and operate at a lower supply voltage (*VDD*) as well. However, since it requires both *Clk* and *Clkb* signals for its operation, high accuracy timing between *Clk* and *Clkb* is required because the second stage has to detect the voltage difference between the differential outputs of the first gain stage at very limited time.

Masaya Miyahara et al. (2008) investigated "*A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs*" that a low offset voltage, low noise dynamic latched comparator using a self-calibrating technique. The new calibration technique does not require any amplifiers for the offset voltage cancellation and quiescent current. The proposed comparator requires only one phase clock while conventionally two phase clocks were required leading to relaxed clock. The comparator without offset Calibration technique resolved this problem by replacing *Clkb* signal with the differential outputs of the first gain stage. As a result, *Clk* load was lessened and the input-referred offset was reduced as well since the gain for the output-latch stage was improved.

However, the current drivability of the output load was weakened (and hence increased delay) because *Clkb* signal was replaced with the output signal of the first Gain stage that has a slower edge rate than *Clkb* and the maximum drive current for each output was reduced.

Ili Shairah Abdul Halim et al. (2011) discussed the design and analysis of a latching comparator using charge sharing circuit topology for low power and high speed. This topology combines the good features of the resistive dividing comparator and the differential current sensing comparator. This design has focused on the minimization of propagation delay and the power dissipation of the comparator, which will improves the comparator performance.

3 Circuit Details

A high speed latched comparator using positive feedback based back to back latch stage, suitable for pipelined Analog to Digital converter, with reduced delay and high speed is proposed.

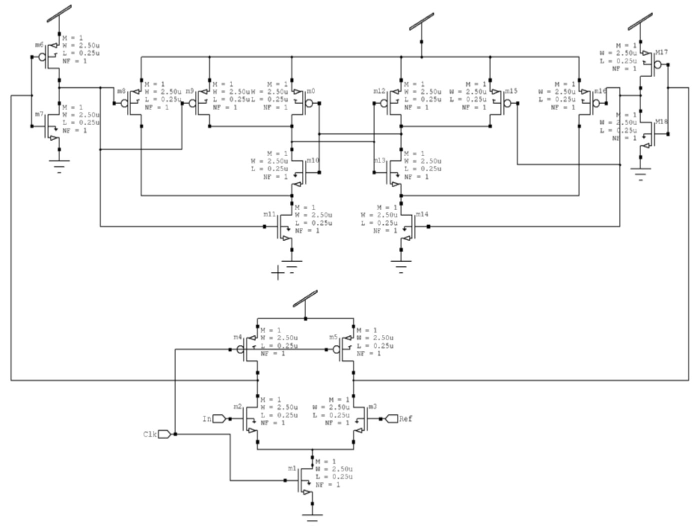

Fig. 1: Latched Cmos comparator.

Differential circuit techniques have become common in many areas of analog circuit design. They are especially useful in rejecting common mode noise in integrated circuits that perform both analog and digital signal processing.

4 Simulation

Comparator design shows reduced delay and high speed with a 1.0 V supply. Finally simulation results of the comparator are given below, when a differential signal is applied as an input to the latched comparator. The simulated results are shown below:

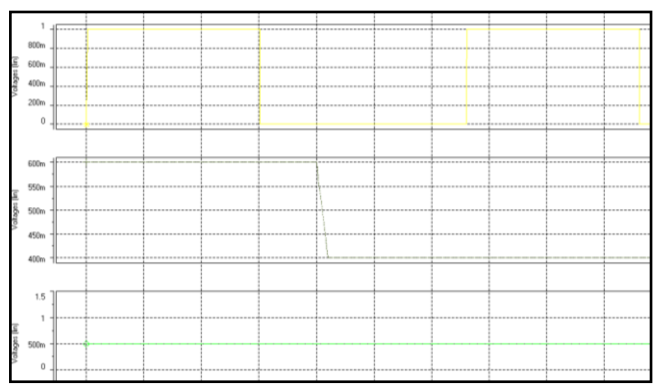

Fig. 2 : Simulation Results (Waveform 1 shows the clock signal applied, waveform 2 shows the analog input applied to the comparator, waveform 3 shows the reference input voltage fixed at 0.5V)

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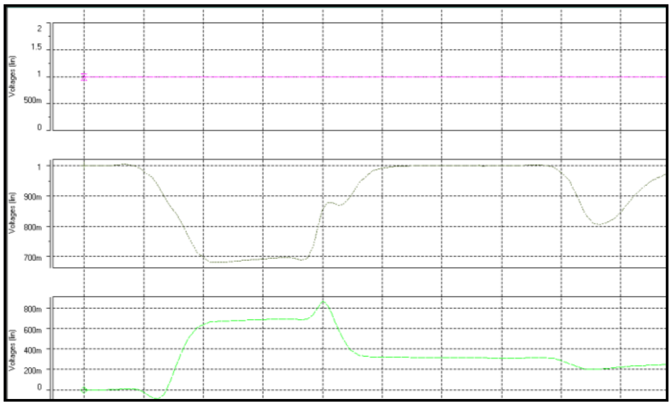

Fig. 3: Simulation Results (Waveform 1 shows the applied suppy voltage of 1.0V, waveform 2 shows the input at the inverter, waveform 3 shows the output of the inverter)

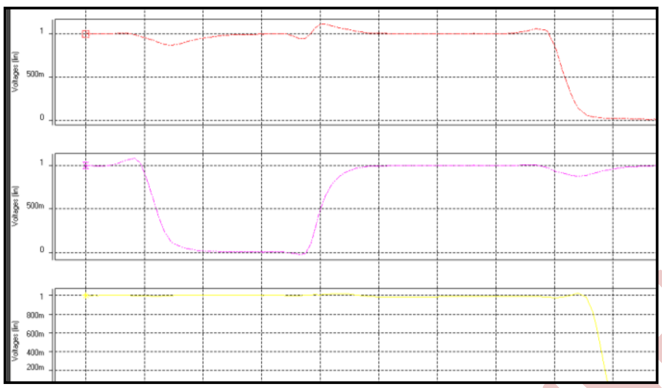

Fig. 4: Simulation Results (Output waveforms of latch stage and final output of the differential stage.)

5 Experimental Results

The overall propagation delay of the above circuit comes out to be 4.378e-10 seconds; the speed of the clock is 3GHZ. Since it shows a reduced Delay, it can be used for fast conversions like Flash ADC's.

TABLE: RESULTS OBTAINED

Circuit Design	Number of Transistors	Clock Speed (GHZ)	Delay (Seconds)	Technology
Figure no 1.	27	3	4.378e-10	CMOS

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REFERENCES

[1] D. Schinkel, E. Mensink, E. Kiumperink, E. van Tuijl and B. Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *ISSCC Dig. Tech. Papers*, pp. 314- 315 and 605, Feb. 2007.

[2] Ili Shairah Abdul Halim, Nurul Aisyah Nadiah Binti Zainal Abidin, A'zraa Afhzan Ab Rahim."Low Power CMOS Charge Sharing Dynamic Latch Comparator using 0.18µm Technology" IEEE, 2011.

[3] T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, pp. 523-52, April 1993.

[4] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1148-1158, July 2004.

[5] Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in *Proc. A-SSCC*, pp. 269-272, Nov. 2008.

[6] Smriti Shubhanand, Dr. H.P.Shukla, A.G.Rao "Design and Simulation of a High Speed Cmos Comparator", International Journal of Electronics and Communication Engineering, ISSN 0974-2166, Vol 6, pp 75-80, 2013

[7] Ili Shairah Abdul Halim, Nurul Aisyah Nadiah Binti Zainal Abidin, A'zraa Afhzan Ab Rahim "Low Power CMOS Charge Sharing Dynamic Latch Comparator using 0.18µm Technology" IEEE, 2011.

[8] Smriti Shubhanand_, Rumaisa Alam, Neha Singh, Kshama Singh, Pallavi "Design of a Three Stage Comparator for High Speed Conversion using CMOS Technology", International Journal of Engineering Research and Technology**,** ISSN 2278-0181, Vol 3, Issue 4 (2014).

[9] B. Murmann et al., "Impact of scaling on analog performance and associated modeling needs," *IEEE Trans. Electron Devices,* vol. 53, no. 9, pp. 2160-2167, Sep. 2006.

[10] Behzad Razavi, *Design of CMOS Analog Integrated Ckts*, Mc-Graw Hill College, 2001.

[11] A.S .Sedra and K.C.Smith, *Microelectronic circuits*, 5th edition Oxford University Press, 1998.