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Active Power Factor Correction of Single-Phase Using Boost Converter Controlling

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Abstract:

This thesis deals with the topic active single phase power factor correction circuits to be used in various applications. The boost-type power factor correction topology was simulated using Matlab/Simulink with a simplified dynamic model of the current stage. Power factor is the ratio of real power (kilo Watt) which is actually consumed by the equipment, to apparent power (kilo Volt Ampere) which is what must be supplied by the network. Power Factor is a measure of how effectively your system uses its electricity supply. A system with poor power factor draws more apparent power than real power. A low power factor is classed as less than 0.9. Certain loads such as inductive loads and capacitive loads reduce the value of this factor.

The efficiency of (Alternating Current-Direct Current) and Direct Current-Direct Current) power converters that are used in many applications like Interruptible Power Supplies (UPS), inverter depends on power factor. Rectifiers used for (Alternating Current-Direct Current) conversion have high harmonic content, low power factor, low efficiency and large size of inductors and filters. Performance and efficiency of converters is increased by high power factor and low line current distortion. This requirement is usually satisfied by incorporating some form of PFC circuits to shape the input phase currents.

In this thesis the conventional AC-DC converter is derived by MOSFET firing angle scheme to control the output voltage and current for capacitive load. These converters have a poor power factor. To increase the power factor PFC converters have been developed by using PWM techniques to achieve a THD of around 94 %. This simulation was implemented in the MATLAB Simulink environment and satisfactory results were obtained.

1. Introduction

There are inherent mechanisms in diode rectification systems which cause these systems to produce severe distortion of the input current and, consequently, a poor power factor (PF). These problems arise because the rectifier diodes are backward biased for a large amount of the line voltage period. This leads to the fact that the current is only drawn when the instantaneous input voltage surpasses that of the output capacitor. Thus, the current will be a “pulse” which is centered around the peak value of the input voltage, this current pulse will act to charge the capacitors. Moreover, the output voltage is directly proportional to the input peak voltage and as such disturbances in the input voltage will be reflected in the output voltage.

Problems with diode rectification may be alleviated by using an active Power Factor Correction (PFC) circuit after the diode rectification bridge - typically a boost converter is used. There is also a possibility to introduce the PFC directly into the rectification bridge. This circuit is controlled so that the inductor current follows a sinusoidal reference to produce an input current which is in phase with the input voltage; thus, emulating the subsequent circuitry as a resistor to the power source. Another great benefit of this set-up is that the output voltage of the rectifier is being controlled independently of line voltage. Previously, PFC-circuits have been incorporated in Switch Mode Power Supplies (SMPS) - e.g. computer power supplies - and these are operated at public grid frequency of 50/60 Hz. These systems have been implemented with varying sophistication depending on cost and application. Cheap consumer electronics may have better displacement power factor but with a relatively high distortion of input current; however, some sensitive electronics may be more sophisticated to reduce harmonics to a very low level (THD < 5%). Research has been done on these kinds of PFC-circuits, and a lot of the applications are designed for 50-60Hz, relatively low power (<1kW) and they are mainly controlled by analog Integrated Circuits (IC). There are standards regulating equipment connected to the grid; for example, IEC61000-3-2 for Europe and IEC555-2/Energy Star Program for USA. According to Nilsson[1] the driving force of these regulations are that the power companies strive to reduce the amount of reactive power into consumer appliances since this is not paid for by the consumers, whom only pay for active power consumed.

The AC/DC power supplies of aircrafts may be fed with a voltage of variable frequency (360- 800Hz), commonly called "wild frequency", which is the cause of the generator being coupled directly to the engine. There are restrictions regarding harmonics in airborne systems. Therefore, it is of great importance to control these to make sure they stay well in range of what might be allowed. This is to make sure sensitive equipment is not affected by the current-harmonics. According to Nilsson the AC/DC power supplies of modern airborne applications functions with a multi-phase transformer which outputs 21 phases from 3 phases to a 42-pulse rectifier. These systems produce very low THD and work very well. However, active Power Factor Correction in a three-phase setting is believed, apart from the obvious reason to reduce THD and PF, to be able to reduce size and weight of the AC/DC converter since no bulky passive components are used in these kinds of systems.

2. Literature review

Cao et al., 2021 [1] illustrated that an active-clamp resonant power factor correction converter with output ripple suppression is proposed and analysed. It combines a buck power factor correction (PFC) unit and a resonant dc-dc unit by sharing one active switch. With another active-clamp switch, a recycling path is built to recover the leakage inductance energy of transformer, which improves the efficiency and the voltage stress of active switch. Therefore, power factor correction can be achieved with inductor current of buck unit operating in discontinuous conduction mode (DCM).

Jing, 2020 [2] discussed that the switched reluctance motor (SRM) suffers the main drawback of torque ripples, and a buck converter-fed SRM motor drive has been proposed to suppress torque ripples and correct a power factor in this paper. An experimental SRM motor drive is formed, and the experimental results show that the proposed drive possesses an improved function with suppression of torque ripples and power factor correction.

Ye and Gooi, 2020 [3] investigates the ability of correcting the power factor at the point of common coupling (PCC) of the source side using dynamic voltage restorer (DVR). By applying the phase angle control (PAC) method, the DVR compensating voltage will be injected with a specific phase angle and magnitude in series with the transmission line, which leads to a power factor angle shift of the resultant load voltage.

Coman et al., 2020 [4] discussed that the equipment connected to the three-phase or single-phase grid, the power factor represents an efficiency measure for the usage of electrical energy. The power factor improvement through correction methods reduces the load on the transformers and power conductors, leading to a reduction of losses in the mains power supply and a sustainable grid system. The implications at the financial level are also important. Given the power factor correction (PFC), the costs are reduced through the elimination of penalties, applying only in the common coupling point (CCP).

Tiwari et al., 2019 [5] discussed that SiC-based diodes and MOSFETs switch extremely quickly with low conduction losses. Thus, from the perspective of efficiency, such devices are ideal for a continuous conduction mode (CCM) boost power factor correction (PFC) converter. The control strategy uses an outer Proportional Integral (PI) controller to normalize output voltage and inner PI controller to shape the input current. PI controller parameters are determined using Tyreus- Luben method.

3. Single Phase Power Factor Correction Topologies

While not technically being a “topology” there is still a way of improving the power factor of the diode bridge rectifier using passive components on the input, namely inductors and capacitors. The addition of a inductor on the ac-side helps to increase the power factor by making the current waveform better; however, the resulting power factor is not perfect. By only providing passive PF-correction the output voltage remains uncontrolled and dependent on the input voltage. To make the output voltage controllable there are some different topologies that can be used depending on the need of either increasing or lowering the output voltage.

The buck-converter topology in Figure 3.2 works in a way that it decreases the output voltage compared to the input voltage. Due to the criteria of having an input voltage greater than the output voltage to work properly this makes the buck-topology a bad choice for a pre-regulator because of the inability to work in the skirts of the half input sine wave having V_{in} less than V_{out}. On the other hand having a buck converter connected after for example a boost pre-regulator makes it a great choice for lowering the “constant” DC voltage or providing a current limiting feature.

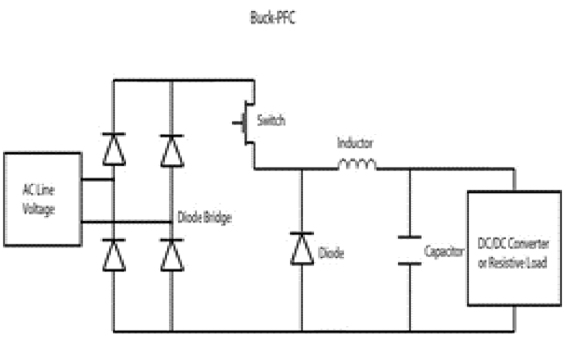


Figure 3.2 Buck PFC topology

Compared to the buck-converter, the boost converter in Figure 4 boosts the output voltage compared to the input voltage. The Boost-PFC topology is the most used and preferred topology in PFC-circuits and one of the reasons to this is the ability to control the input current. Criteria’s for making a boost-converter work in a convenient way is that the output voltage is higher than the input voltage. If the circuit is constructed in such a way that the output voltage exceeds the maximum peak of the input voltage it will be able to work in the full range from zero to max peak value. Due to the ability to work at high power levels and the possibility to use current mode control to program the input current half sine wave it makes the boost topology a popular choice. If the converter works in Continuous Conduction Mode (CCM) the inductor- and input current will always be continuous, helping to reduce input current harmonics. If there is a need to have lower voltage levels it is often popular to have a buck converter connected in series with the boost to make this transformation instead of having a buck right from the start. One drawback with the boost topology is that it does not have a switch in series between the input and output, therefore it is unable to limit the input current. This means overload and/or startup currents cannot be controlled. Also, if the input voltage surpasses that of the output voltage the converter is unable to control the current as the diode will be forward biased and the current will flow continuously.

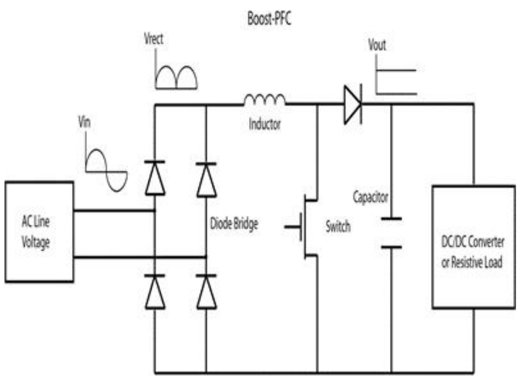
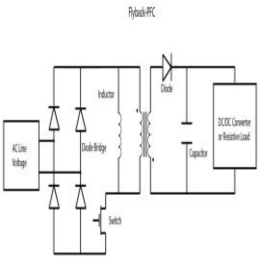


Figure 3.3 Boost PFC circuit

When it comes to the feature to both be able to have the possibility to create a higher and a lower output voltage compared to the input voltage there are some different converters that can be used. This can come in handy when there is a special need for the circuit to be able to do both conversions without using two different converters connected in series. Two common converters are the Buck/Boost-converter and the Flyback-converter. The mentioned features make these topologies viable choices compared to only a Buck or Boost. The basic concept of the two is the same but they are constructed in two different ways that will be described further down. Examples of simple schematics that are most common for the converters are shown in figures 3.4 and 3.5 below.

Several different approaches are possible when constructing Buck/Boost and Flyback- converters. In the Buck/Boost case there are versions where two switches are used instead of the conventional single-switch topology, there are also some topologies involving magnetic isolation i.e. there is a galvanic isolation between the input and output sides. Also, Flyback- converters have the advantage of having low cost and galvanic isolation of the voltage. It is also able to both regulate the output voltage both up and down as mentioned making it a competitively choice when choosing converter topologies for power electronics. Working under optimal conditions Flyback-converters have high efficiency, and that is in power levels <500W. For applications using higher power levels it is required to parallel devices. To achieve this there is also a need to have control algorithms able to perform these tasks, to do this a DSP is optimal to drive the circuit.



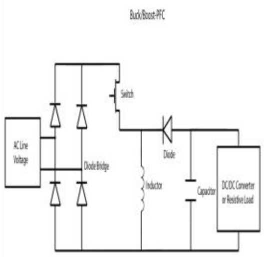


Figure 3.4 Flyback PFC converter Figure 3.5 Buck/Boost PFC

The Buck-, Buck/Boost- and Flyback-topologies have discontinuous input current due to the fact that there are switches in series with the line for these topologies. However, the input current of Boost-topology can have an input current in both CCM and DCM. The ability to operate in CCM makes the Boost-topology the most viable option of the mentioned topologies for high performance power factor correction circuits.

4. Introduction to PSO

PSO calculation depends on swarm intelligence (SI). The strategy got inspiration by noticing the social collaboration, practices of creatures seen among birds, fishes and so on. PSO follows the technique that is found in fishes, where they discover food by contending and the coordinating among themselves. The multitude has people which are considered particles in which every molecule addresses different conceivable arrangement of the boundaries that are obscure which ought to get improved. A 'swarm' is normally instated by a populace of arbitrary arrangements. In this framework, particles fly's around in a multi-dimensional hunt space. It continues changing its situation as for its own insight and furthermore by thinking about the experience of its adjoining molecule.

The objective of every molecule is to look through an answer effectively to accomplish this. The particles swarm among themselves and moves to the best capacity which is called fitting capacity. At that point it unites to a solitary min or max arrangement. A capacity is now characterized and that capacity is utilized to examine the presentation of that molecule. The precision of the regulator that is tuned relies upon model's exactness. So, the framework model is significant. The lone target of this work is to utilize the proposed PSO to accomplish the ideal boundary estimations of a PID regulator that is utilized in a two-tank process. Here we instate a framework with a populace that has arbitrary arrangements. They are called particles. Furthermore, an arbitrary speed is allocated to every one of them. PSO relies upon the data that get traded between swarms (particles). Each multitude adjusts its way to its best wellness work that has been accomplished till that second. This worth is alluded as pbest. In addition, swarms change its way likewise by considering the best past position that was accomplished by its adjoining part. It is alluded as gbest. In the inquiry space the particles move with a speed which is versatile in nature.

A capacity is utilized to break down the presentation of multitude; with the goal that we can discover whether it has achieved the best arrangement. This capacity is called wellness work. As the amassing happens, every molecule attempts to accomplish its best capacity and by the end, particles show a deteriorating pattern. Through this cycle every molecule gets upgraded. Think about D as the component of search space.

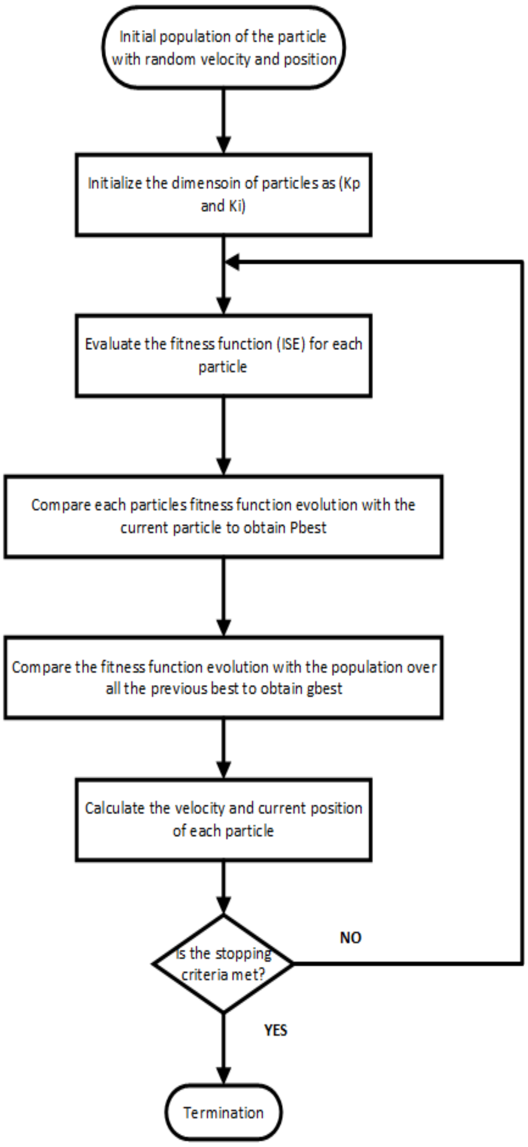


Fig. 2 PSO flow chart

A basic PSO has two phases, exploration and exploitation. In the exploration phase, particles search the most promising regions and in the exploitation phase particle moves towards the best position. PSO finds the global best (gbest) value of particles by changing their position with respect to best position of particles. Local best value (pbest) of each particle communicates their information to the rest of the particles through their neighbors. Therefore, the overall best position of particles attracts the other particles gradually according to the updated velocity of each particle which is depending on gbest and pbest values. The efficiency of the algorithm depends on the strategy used to select parameters for the next iteration. The basic PSO algorithm requires three steps, namely, generation of particles, positions and velocities, second, update velocity and third, position update. PSO is initialized with the group of random particle positions (x_i^k) and velocities (v_i^k) between upper and lower bound of design variable values as expressed in following equations

$$x_i^k = x_{min} + rand(N,d).*(x_{max} - x_{min}) \quad (3.1)$$

And

$$v_i^k = v_{min} + rand(N,d).*(v_{max} - v_{min}) \quad (3.2)$$

Where, *N*: number of population.
d: number of parameters to optimize.
k: current iteration count.
x_{min} and x_{max}: minimum and maximum value of particles in search space.
v_{min} and v_{max}: minimum and maximum value of the position of particles to move in search space.

The second step is to update velocities of all particle positions for next (k+1) iteration using the particles fitness values which is function of particle positions. These fitness function value determines which particle has a global best ($gbest_k$) value in the current swarm (iteration) and also determine the best position ($pbest^i$) of each particle.

After finding the two best values, the particles update its velocity and positions of each (i^{th}) particle using following equation:

$$v_i^{k+1} = wv_i^k + c_1r_1(pbest_i^k - x_i^k) + c_2r_2\,(gbest^k - x_i^k) \quad (3)$$

Where, r_1 and r_2 are the two distinct random values between 0 and 1. c_1 and c_2 are acceleration constant which are set at 2. These constants help to move particles towards the best possible value ($gbest^k$) and '*w*' is the inertia weight used to balance between previous and current best value. Inertia weight change in succeeding iteration as :

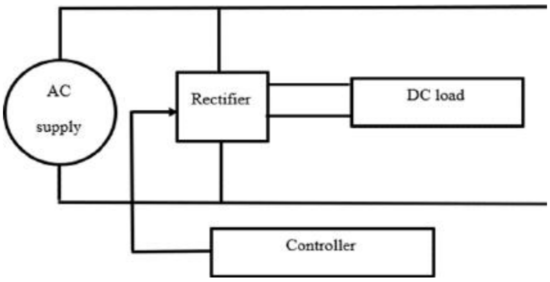
$$w = w_{max} - \frac{(w_{max} - w_{min})}{itermax} * iter \quad (4)$$

Where, itermax is the maximum number of iterations. w_{max} and w_{min}, the upper and lower limit of inertia weights which are 0.9 and 0.4 respectively. Now positions of particles are updated using following equation:

$$x_i^{k+1} = x_i^k + v_i^{k+1} \quad (5)$$

5.RESLT AND DISCUSSION

The following block diagram illustrate the basic model proposed in this project for achieving power factor as high as possible



(a)

(b) Fig. 5.1 Illustrate block diagram for the model

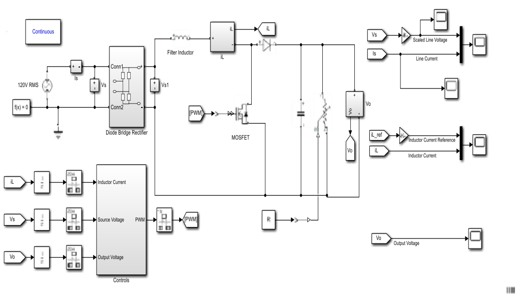


Figure 5.2 Represents MATLAB model for PFC circuit

The voltage source supplies the load with AC voltage. The rectifier is connected in series with the DC load which is represented by a resistance. The rectifier converts the AC voltage into DC voltage. The rectifier consists of controlled MOSFET which are switched ON by a pulse and turned-OFF by natural commutation. The pulse generator provides a pulse signal to turn the MOSFET ON after certain time from the beginning of each half cycle (Firing)and turned-off naturally at end of the half cycle. Controlling the firing angle causes the fundamental component of the current to lags the voltage. The source sees two phase shifts in two different directions (leading and lagging) so the correction (as seen from the source side) is obtained from the effect of the current flowing in the rectifier branch (corrected current) on the total current supplied from the source. The firing angle control in the rectifier affects the source current waveform leading to a higher power factor.

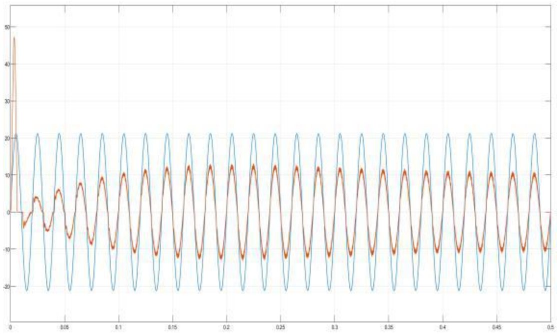


Fig 5.3 Line current across load

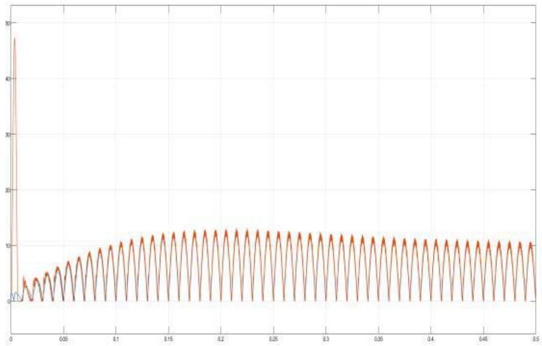


Fig 5.3 Inductor current across load

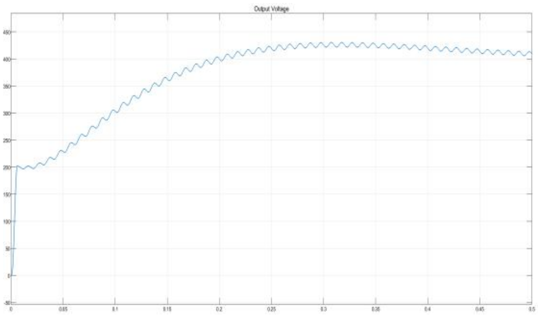


Fig 5.4 Output voltage across load

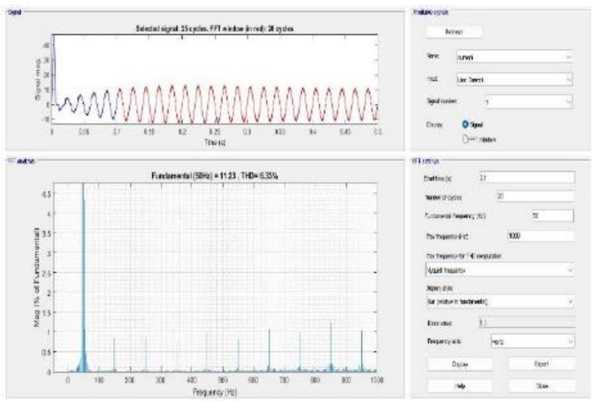


Fig 5.5 THD of model designed

Change in firing angle changes the power factor. when firing angle increases the phase difference between fundamental voltage and current increases and the power factor continue to increase until a certain point where the current is small compared to the total current so the effect of the correction current will be small making the AC effect more obvious to the source.

5. Conclusion

The basic purpose of a Power Factor Correction circuit is to make the line current follow the waveform of the line voltage so that the input to the power supply becomes purely resistive and hence to improve the power factor. Having a poor power factor makes the circuit operate in an inefficient manner leading to energy losses and possible damage to equipment.

The AC load alone has a bad power factor, and when the DC load is used the circuit obtained high values of power factor due to the effect of the DC load. Change in firing angle changes the power factor when firing angle increases the phase difference between fundamental voltage and current lead to variably lagging phase shifts in the fundamental component of the current waveform. So, there is inverse relation between firing angle and power factor of converters.

The power factor of the DC load circuit is high but the circuit still manages toimprove it further proving its effectiveness and the effectiveness of this methodology. PWM based power factor measurement and correction unit can improve the power factor close to unity in an automatic way and can remove the capacitor banks when the power factor is leading**.** The system gives reliable and economic solution for industries and multi-storied building applications.

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